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POWER DEVICES AND SYSTEMS LABORATORY

# Exercise 1F

## Physical Bases of Operation of Power Semiconductor Devices

Blocking High Voltages

Conducting High Currents

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Łódź 2018

ver. 6.1.0 (en). 5/10/2018

## Contents

# B

# Exercise Introduction

## 1. Exercise Aim and Plan

The aim of this exercise is to investigate the physical mechanisms used in power semiconductor devices to block high voltages and conduct high currents. The analysis will be performed based on the example of the simplest semiconductor device: the diode. Nevertheless, conclusions from this exercise may be extended to all the power semiconductor devices. This is because each of them contains in its structure a layer set analogous to one of the analysed diodes.

Using simple models implemented in a spreadsheet, SBD (Schottky Barrier Diode, unipolar) and PIN (bipolar) power diodes will be analysed. The effects of semiconductor structure technological parameters on electrical properties will be determined for either device. Both diodes will then be compared one to another in respect of their voltage and current capabilities.

To simplify, only the parameters of the lightly doped layer, crucial for power semiconductor device operation, will be considered: width, dopant concentration and (for the bipolar device) carrier lifetime. The blocking state and the conducting state will be considered separately, but it the end, final conclusions will be drawn taking both into account.

Using computer models and tools will enable virtual investigation of multiple devices with various technological parameter values in a short time and without the need to use high-end measurement equipment indispensable in atomic-level research on semiconductor materials.

# 2. Power Diodes

## 2.1. Recommended reading

| Ref. | Textbook | Excerpt | Equivalent in the Polish Manual | Complementary Reading | Complements in this Manual |
|---|---|---|---|---|---|
| A | Ben | 5, 5.1 | 2.1.a—b; #0 6.2.d, 6.5, 6.6 | | |
| B | Ben | 5.2 | 2.1.c; #0 5.2.e, 5.3.b, e—f | | |
| C | Ben | 5.3, 5.3.1, 5.3.2 | 2.2; #0 6.7.b | | |
| D | Ben | 5.4 | 2.3; #0 5.4.c, 6.1.e, 6.7.a | | |
| E | Ben | 5.5, 5.5.1, 5.5.2 | 2.4.a | | |
| F | Moh | 20-3, 20-3-1, 20-3-2 | 2.1.c; #0 5.2.c—f, 5.3.a—b, e—f | | 3.2 |
| G | Moh | 20-4-2 | #0 6.1.e | | |

Additionally, from Manual 0 references:

| Ref. | Textbook | Excerpt | Equivalent in the Polish Manual | Complementary Reading | Complements in this Manual |
|---|---|---|---|---|---|
| 0 H | Ben | 3.1.1 | 2.1.a, 2.3.a | | |

# C

# Experiment

## 3. Simulations

### 3.1. Investigation of the PIN diode in reverse blocking state

#### Using the spreadsheet

This part of exercise should be carried out using the worksheet *pin_stan_zaworowy.ods*, which should be copied to the team's account.

The worksheet contains one spreadsheet, displaying the electric field distribution $E(x)$ along the PIN ($P^+N^-N^+$) diode. The word "distribution" means a graph showing values of a given physical quantity in various points of the space. In the considered, simplified case the space is one-dimensional: it is limited to the $x$-axis which is identified as the anode-cathode line (see Ref. B, Fig. 5.7). Thus, the distribution curve $E(x)$ shows how strong electric field is at a given point of the diode (defined by the distance $x$ from this point to the anode).

The electric field distribution in the given semiconductor structure depends on the following parameters visible in the spreadsheet window:

(1) general constants and physical parameters, such as:
- $e$ – electric charge of an electron,
- $\varepsilon_{Si}$ – relative permittivity of silicon,
- $\varepsilon_0$ – absolute permittivity of vacuum,

(2) technological parameters of the device, namely:
- **$N_D$ – dopant concentration in the lightly doped layer,**
- **$W_I$ – width of the lightly doped layer (base),**
- $N_{D+}$ – dopant concentration in the emitter layer $N^+$,
- $N_{A+}$ – dopant concentration in the emitter layer $P^+$;

2) device operating conditions which in the case of reverse bias can be limited to:
- **$U_R$ – reverse bias voltage applied across the structure.**

The parameters intended to be changed by the student are marked above and in the spreadsheet by the bold font. The remaining parameters should not be changed. It is best to confirm the new value by using the key combination *Alt+Enter* because the cursor will not move to the next cell then.

To facilitate determination if avalanche breakdown or punch through occurs in the structure, there are two lines visible in the graph:

- $E_{\mathrm{crit}}$ – indicating the level of the critical electric field,
- $W_{\mathrm{I}}$ – indicating the end of the lightly doped layer.

Additionally, below the $U_{\mathrm{R}}$ value there is a field where one of the following messages is displayed:

- *Applied* – if the entered voltage value can appear across the device,
- *Impossible* – if it is not physically possible for the entered value voltage to appear across the device because at a lower voltage the device would already enter breakdown state, which would make it conduct a very high current that would cause opening of the circuit due to one of its elements breaking down.

Based on the input parameters, not only the field distribution is drawn, but also the following values are computed:

- the critical electric field $E_{\mathrm{crit}}$,
- maximum electric field along the $x$ axis $E_{\mathrm{max}}$,
- the width of the space charge regions in the subsequent layers – $W_{\mathrm{sc(P+)}}$, $W_{\mathrm{sc(N-)}}$ and $W_{\mathrm{sc(N+)}}$.

Depending on parameter values, the displayed structure may represent a device with or without punch through. These are often referred to as non-punch-through (NPT) and punch-through (PT) devices, respectively. However, another classification defines punch-through devices as *invulnerable to punch through*, and not those with *punch through occurring* during their operation. These two approaches can give equivalent results but this is not always the case. For example, the PIN diode is invulnerable to punch through by its semiconductor structure but it can be manufactured as a wide-base device where punch through does not have any possibility to occur; depending on the definition chosen, such a device can be classified as NPT or as PT. Therefore, to avoid misunderstanding, we will not use the common abbreviations NPT and PT, with the exception of symbol subscripts. Instead, we will refer to the analysed structures as to "without punch through" and "with punch through" meaning "where punch through occurs during operation" and "where punch through does not occur during operation."

### Saving graphical results

Performing tasks should be documented by saving the obtained graphs together with parameter values for which they have been obtained. For this purpose you must use the *(Copy) All* button, which copies the appropriate spreadsheet fragment to the clipboard. For the *Copy* button to work correctly, the spreadsheet window must be the active one when this button is pushed.

For the *Copy* buttons to work, macros must first be enabled, which are disabled by default in the LibreOffice package. This can be done from the menu *Tools* ▸ *Options* ▸ *LibreOffice* ▸ *Security* ▸ *Macro Security* by setting the security level to *Low*. After this change is made, the worksheet has to be closed and reopened.

Graphs should be copied to the text document in the following way:

- from the menu, choose *Edit* ▸ *Paste special* or press *Ctrl+Shift+V*;
- choose the *Bitmap* option and accept;
- click with the right mouse button on the graph pasted;
- from the context menu, choose *Anchor* ▸ *As character*;
- should the change in anchor result in the image moving to a wrong location, select the image by a single click on this image, then cut (*Ctrl+X*) and paste (*Ctrl+V*) in the appropriate line.

## Creating tables and graphs

Apart from the graphical form, results so indicated in the notes template should be saved in the numerical form by placing them in tables based on which synthetic characteristics of electrical quantities have then to be obtained and inserted. A separate spreadsheet, *pin_stan_zaworowy_wyniki.ods*, is available for this purpose.

Numerical results should be copied from the basic spreadsheet (*pin_stan_zaworowy*) to the results spreadsheet (*pin_stan_zaworowy_wyniki*) in the following way:

- in the basic spreadsheet, click *(Copy) Numbers*;
- in the results spreadsheet, select the first cell in the appropriate row of the table at the top of the sheet;
- choose *Edit* ▸ *Paste special* or press *Ctrl+Shift+V*;
- check only the *Numbers* option (especially, the *Formulas* option should be unchecked) and accept.

Tables and graphs should be copied from the results spreadsheet to the notes template in the following way:

- from the menu, choose *Edit* ▸ *Paste* or press *Ctrl+V*;
- click with the right mouse button on the table or graph pasted;
- from the context menu, choose *Anchor* ▸ *As character*;
- should the change in anchor result in the table or image moving to a wrong location, select the image by a single click on this image, then cut (*Ctrl+X*) and paste (*Ctrl+V*) in the appropriate line.

## Carrying out simulations and analysing results

1. Enter your team number and academic year into the appropriate spreadsheet fields.

   **Submitting results without the above fields filled in will be considered as cheated.**

2. From the web page, obtain and enter into the appropriate fields the initial values of the lightly doped layer parameters:
   - dopant concentration $N_{D,ini}$,
   - width $W_{I,ini(B)}$.
3. Obtain and analyse results according to the directives found in the notes template.

## 3.2. Investigation of PIN and SBD diodes in forward conducting state

### Electric potential distribution

This part of exercise should be carried out using the worksheet *pin_sbd_stan_przewodzenia.ods*, which should be copied to the team's account.

The worksheet contains one spreadsheet where three distributions along the $x$ axis, i.e., along the anode to cathode line, are plotted for two power diodes, a PIN and an SBD (Schottky) one:

- $p(x)$, hole concentration distribution,
- $n(x)$, electron concentration distribution,
- $V(x)$, electric potential distribution assuming that the potential of the negative electrode, i.e., the cathode, is zero.

The first two distributions demonstrate what is the concentration of carriers of a given type (i.e., how many of them are contained in a unit volume) at a given distance $x$ from the anode.

The latter distribution shows the **electric potential of a given point relatively to the zero electric potential point**. (Remind that a electric potential value is always relative and depends on which point we assume to have the potential of zero.) As indicated above, in the considered case the lowest potential within the diode, i.e., one of the cathode, is assumed to be zero.

Moreover, electric potential difference between any two points equals the voltage between these points:

$$V(x_2) - V(x_1) = U_{21} \tag{3.1}$$

Therefore, the **difference between the values of $V(x)$ read out at both ends of a given region** (e.g., emitter layer, charge storage region, junction etc.) tells us how large a **voltage drop is induced across this region by the flowing current**. In the extreme case, the difference between the anode potential and the cathode potential, i.e., the difference between the values at the left and right ends of the curve is equal to the total voltage drop across the diode in the conducting state.

Observation of the $V(x)$ distribution allows us to determine:

1° what the **total voltage drop** $U_F$ across a diode with given parameters and under given current density is: according to the above ($V_K = 0$), it equals the anode electric potential $V_A$;

2° what the **contributions of the particular components** (see Refs. A and D) are to this total voltage drop.

Additionally, the shape of the distribution curve in a given layer indicates the **character of conductivity**. In layers exhibiting unipolar (drift) conductivity, the resistivity $\rho(x)$ is constant, so across every elementary section $\Delta x$ the same voltage will be dropped, equal

$$\Delta U = \rho(x) \cdot \Delta x \cdot J \tag{3.2}$$

which implies the linear character of the electric potential distribution curve.

On the other hand, in layers exhibiting bipolar conductivity (drift and diffusion), the resistivity $\rho(x)$ at every point of the lightly doped layer depends on the concentration of excess carriers at this point. As this concentration varies along the $x$ axis then according to the above equation, across different elementary sections $\Delta x$ we will observe different elementary voltage drops. Thus in this case, the character of the electric potential distribution curve will be non-linear.

## Using the spreadsheet

The distributions plotted in the spreadsheet depend on the following parameters visible in the window:

(1) general constants and physical parameters:
- $e$ – electric charge of the electron,
- $\mu_n$ and $\mu_p$ – electron and hole mobilities,
- $n_i$ – intrinsic semiconductor equilibrium carrier concentration,
- $k$ – Boltzmann constant,
- $D_n$, $D_p$, $D_a$ – electron, hole and ambipolar diffusion constants,
- $A^*$ – Richardson constant;

(2) technological parameters of the device:
- **$N_D$ – dopant concentration in the lightly doped layer,**
- **$W_I$ – lightly doped layer width,**
- **$\tau$ – minority carrier lifetime in the lightly doped layer (only applicable to the PIN diode),**
- $A$ – the cross-section perpendicular to the anode-cathode axis,
- $N_{D+}$ and $W_{N+}$ – dopant concentration and the width of the $N^+$ layer ($W_{EN}$ or $W_{SN}$), respectively
- $N_{A+}$ and $W_{P+}$ – dopant concentration and the width of the $P^+$ layer (only for the PIN diode),
- $\varphi_B$ – the potential of the energy barrier in the Schottky junction (only for the SBD diode),
- $N_{Al}$ and $t_M$ – electron concentration for aluminium and the thickness of the metal electrode (only for the SBD diode);

(3) device operating conditions which in case of the forward conducting state can be limited to:
- **$I_F$ – current forced through the structure.**

Parameters intended to be changed by the student have been marked above and in the spreadsheet in bold type. The remaining parameters should not be changed. It is best to confirm a new value with *Alt+Enter* because the cursor will not move to the next cell then.

To avoid obscuring the picture of phenomena and allow the most thorough observation possible of the key lightly doped $N^-$ layer, the distributions are plotted with the assumption of the abrupt character of the junctions, i.e., the voltage drop across the junction occurs at an infinitely small distance $\Delta x$. Moreover, the heavily doped $N^+$ layer can be shown cut from its right-hand side to avoid the inconvenient change of scale of the $x$ axis (which would make a precise distribution analysis in the $N^-$ layer impossible).

To facilitate the analysis of the total voltage drop across the diode as well as of the contributions of its individual components, the spreadsheet computes and displays:
- the total voltage drop across the diode $U_F$,
- voltage drop components of $U_M$, $U_J$, $U_I$ and $U_S$ for the SBD diode,
- voltage drop components of $U_{EP}$, $U_{JP}$, $U_I$, $U_{JN}$ and $U_{EN}$ for the PIN diode,
- the resistance of the lightly doped layer $R_I$.

## Saving and processing results

Performing tasks should be documented by saving the obtained graphs together with parameter values for which they have been obtained using the *(Copy) All* button. To accomplish this you should proceed as described in section 3.1 (under “Saving graphical results”). Saving graphs for both

diodes at the same time, which is possible using the *(Copy) All* button, will make their later comparison easier.

Apart from the graphical form, results so indicated in the notes template should be saved in the numerical form by placing them in tables based on which synthetic characteristics of electrical quantities have then to be obtained and inserted. A separate spreadsheet, *pin_sbd_stan_przewodzenia_wyniki.ods*, is available for this purpose. The above procedures are analogous to the ones described in Section 3.1 (under "Creating tables and graphs").

## Carrying out simulations and analysing results

1. Enter your team number and academic year into the appropriate spreadsheet fields.

   **Submitting results without the above fields filled in will be considered as cheated.**

2. From the web page, obtain and enter into the appropriate fields the initial values of:
   (a) the lightly doped layer parameters:
      - dopant concentration $N_{D,ini}$,
      - width $W_{I,ini(A)}$ (a new one, different from the one used in Section 3.1),
      - minority carrier lifetime (for the PIN diode) $\tau_{ini}$;

   (b) conduction current $I_{F,ini}$.
3. Obtain and analyse results according to the directives found in the notes template.

# E

# Information

## 4. Required Knowledge

### 4.1. Prerequisites

**First part**

- Electric field distribution at a reverse-biased PN junction. Avalanche breakdown condition. Punch through condition.
  (Refs. B and F; lecture)
- Voltage and current waveforms during PIN diode reverse recovery. Reverse recovery time.
  (Ref. C)

**Second part**

- Carrier concentration and voltage drop across a semiconductor layer in the case of drift only and in the case of drift and diffusion.
  (Ref. A and Manual 0, Refs. I and J)
- PIN and SBD diode structures (cross-section).
  (Manual 0, Ref. H)

## 5. References


Benda V., Gowar J., Grant D. A.: *Power Semiconductor Devices: Theory and Applications.* Wiley, 1999. ISBN 0-471-97644-X.

Mohan N., Undeland T. M., Robbins W. P.: *Power Electronics: Converters, Applications, and Design.* 3rd Ed. Wiley, 2003. ISBN 0-471-22693-9.