



POWER DEVICES AND SYSTEMS LABORATORY

# Exercise 7K

## **Design and Prototyping of a Switched- Mode Power Converter**

### **Buck DC Converter**

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Łódź 2019



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## Course Introduction

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### 1. Electronic circuit components

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#### 1.1. Selected electronic components

Fig. 1 presents photographs of selected typical electronic components of the kinds that will be used in the circuit to be designed and assembled in this exercise.

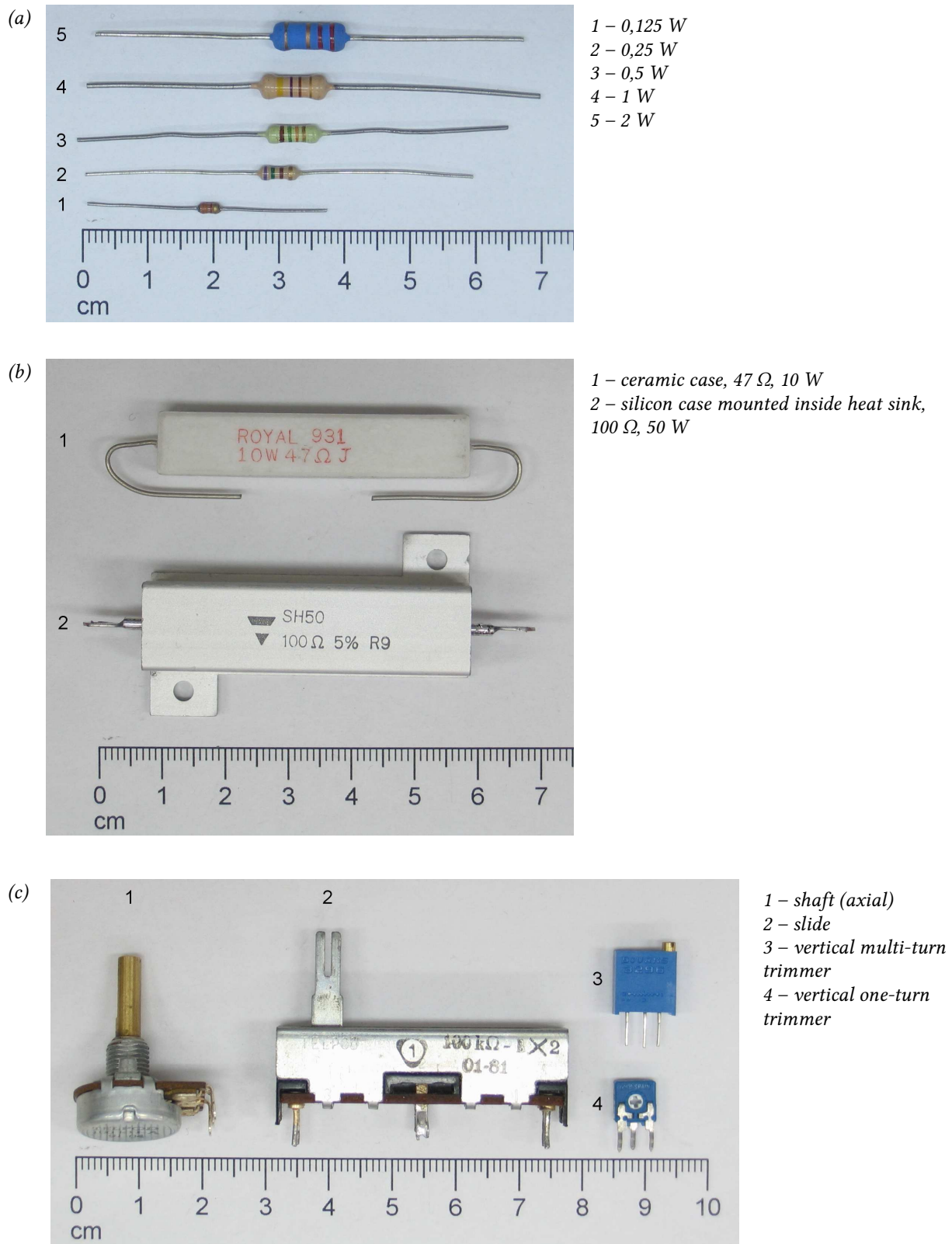


Fig. 1. Electronic components  
 (a) low power resistors; (b) middle power resistors; (c) potentiometers



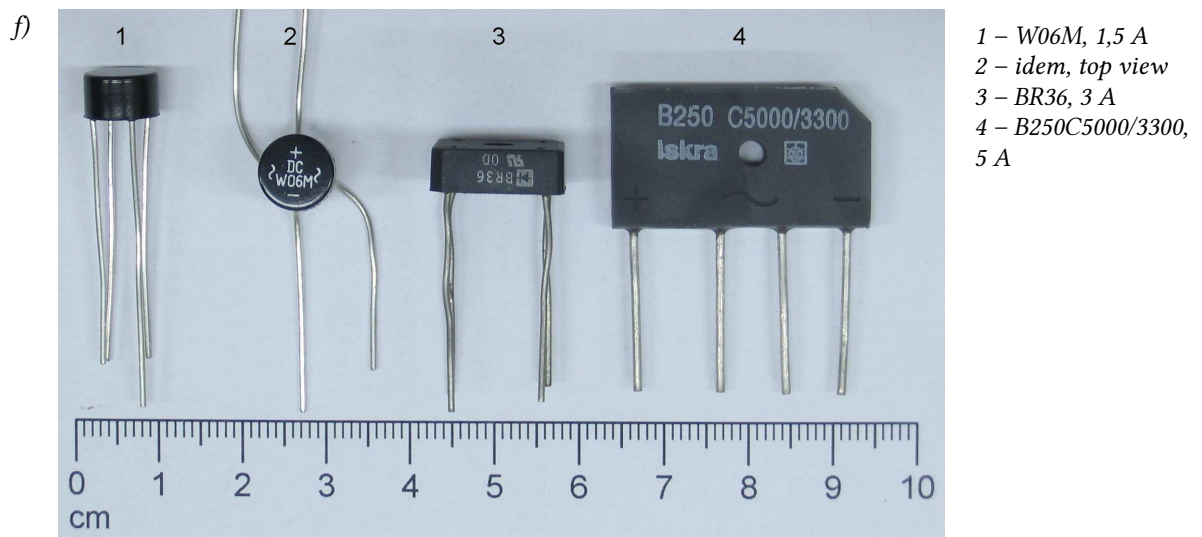
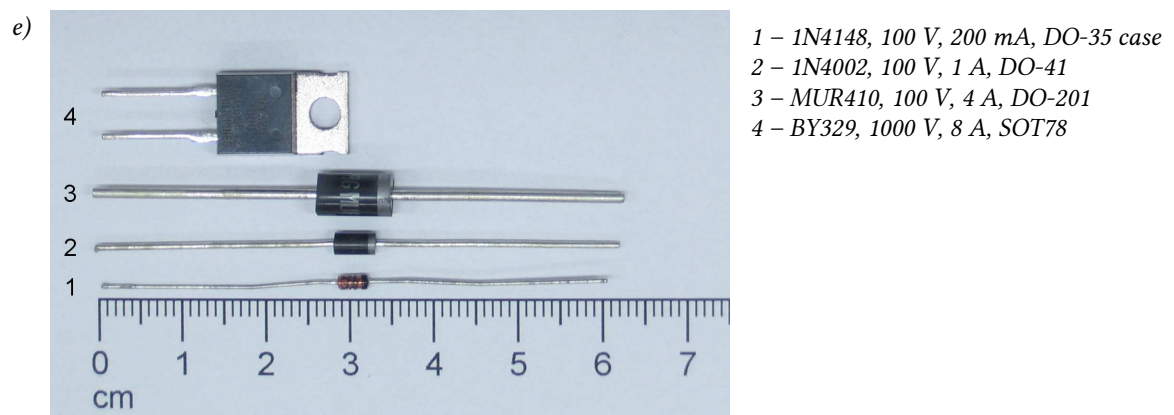
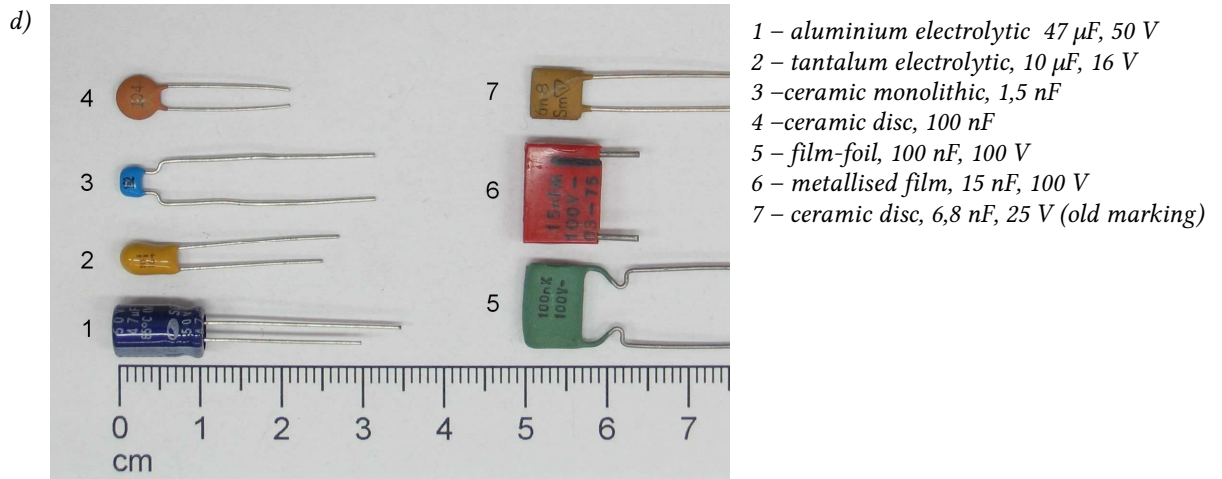


Fig. 1 (cont.) Electronic components  
 (d) capacitors; (e) diodes; (f) rectifier bridges

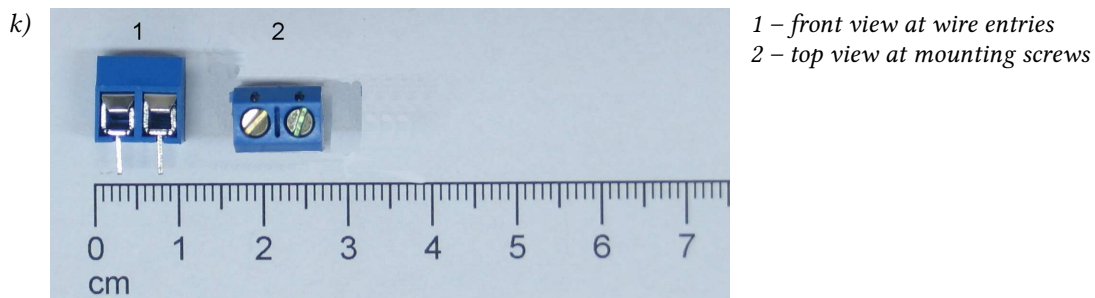
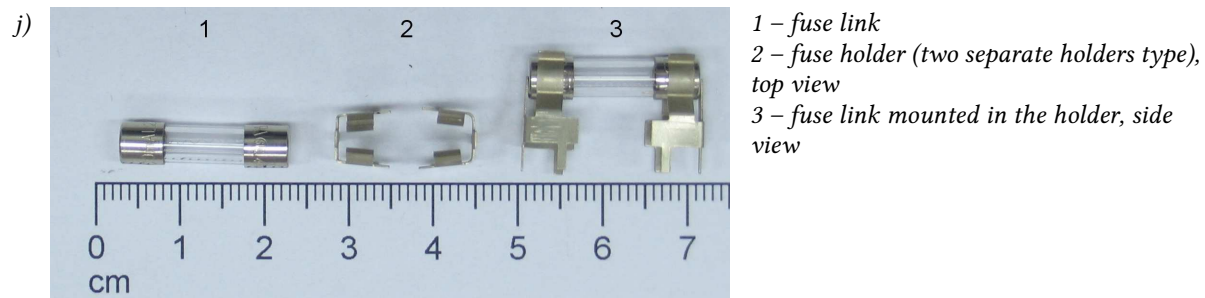
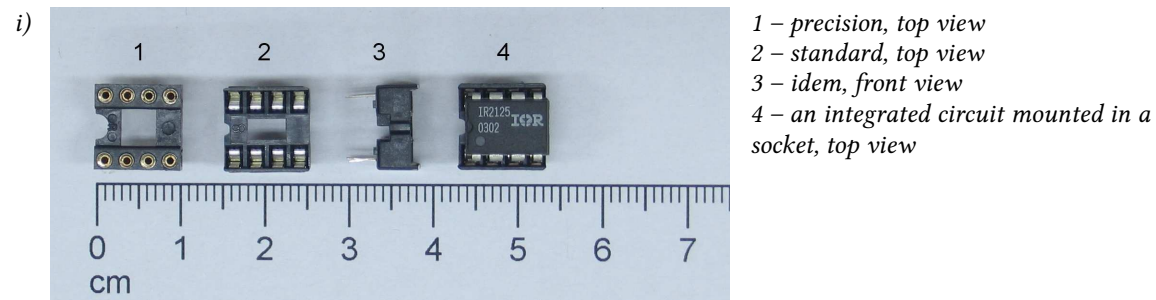
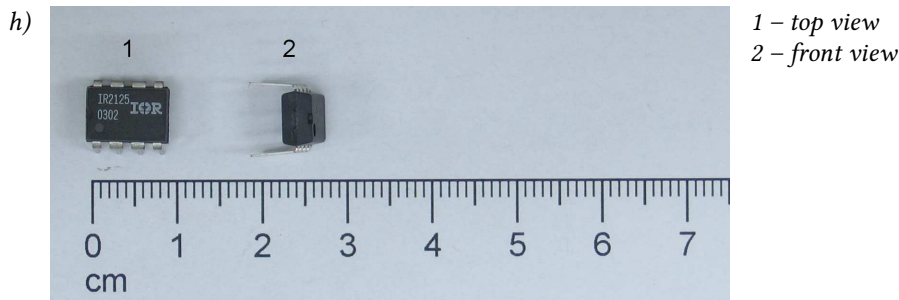
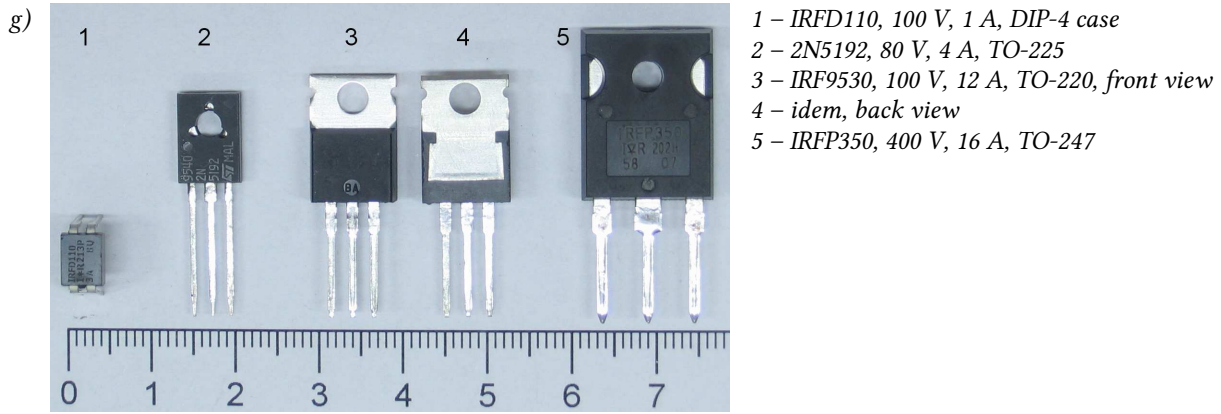


Fig. 1 (cont.) Electronic components

(g) power MOSFETs; (h) integrated circuit (IR2125, DIP-4 case); (i) integrated circuit socket; (j) IEC standard fuse (3,15 A, 250 V, 35 A breaking capacity); (k) terminal block, horizontal wire entry

## 2. Printed Prototype Circuit Boards

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### 2.1. Universal printed circuit boards

#### 2.1.a. Board structure

For the prototyping of the physical circuit, a **universal prototyping printed circuit board** (*universal PCB*) may be used. It is a flat piece of laminate (a plastic made of two different materials), 1 to 2 mm thick, with pre-drilled (frequently at equal distances) **mounting holes** and pre-manufactured (usually one-sided) **solder pads** (the metallisation surrounding the hole, enabling to solder a component's lead or a conductor). Mounting holes are frequently pre-connected with regularly placed metallic **conducting traces**.

As such a board may be used to prototype an arbitrary circuit, it is called 'universal.' Universal PCBs are frequently used for circuit prototyping to avoid the time-consuming PCB design, etching and drilling where it is very likely for the circuit idea still to change multiple times.

Fig. 2 presents a view of an exemplary universal prototype PCB. It is a **single sided** PCB, i.e. with metallic traces manufactured on its one side only (which makes it different from the *double sided* PCBs), where solder pads have been pre-connected. This board has a **lead pitch** of 2.5 mm which means that holes and pads (where component leads may be soldered) are placed at the nodes of a 2.5-millimeter square grid.

Trace layout is similar on most universal PCBs. Multiple short vertical connections are manufactured (the vertical and horizontal directions obviously being conventional). Above and below them, longer horizontal traces are realised that are commonly used to distribute power supply and ground to the particular components. Such traces may also be placed vertically, sparsely distributed in the interior or along board edges (the latter being the case of Fig. 2). A board with such a trace layout is well suited for the present exercise.

A universal PCB may be partitioned into several separate sub-circuits. For example, on the board presented in the photograph, 2 separated sub-circuits can be seen (in its left-hand and right-hand sides). Moreover, each of the sub-circuits has two separate connection rows along two horizontal double middle lines (in the upper and lower board quarter). For these rows, only the long vertical trace along the board edge is common.

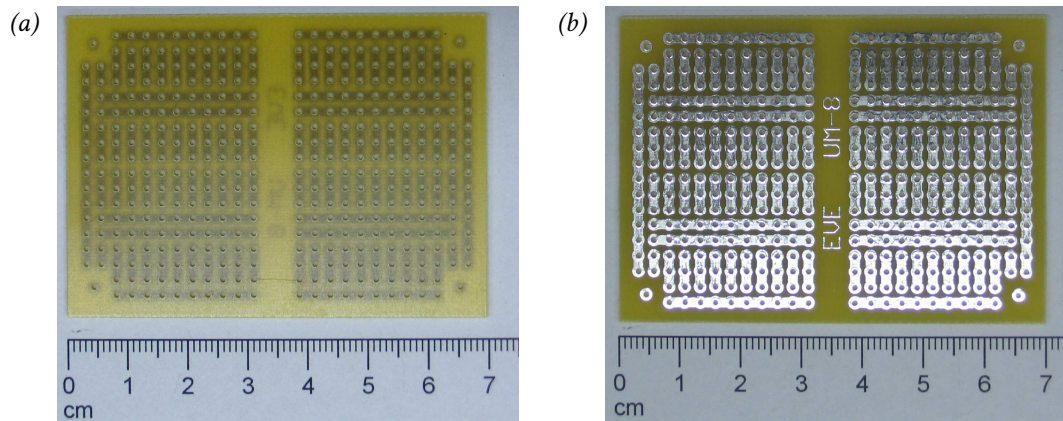


Fig. 2. Single sided universal PCB with pre-connected solder pads  
(a) component side; (b) solder side

As already mentioned, a PCB that has metallisation realised only on its one side is called a single sided PCB. The side on which connections have been manufactured is called the **solder side** whereas the other is the **component side**. Components are essentially placed on the component side (although this is not always the case, especially when a component has to be added). Soldering is done on the solder side.

In the present exercise, the circuit will be realised using the **through-hole technique** (or **through-hole mount**). This term means that component leads are passed through mounting holes to the solder side where they are soldered to solder pads. This technique is very well suited for circuit prototyping because of high soldering speed and the lack of high precision and special care requirements.

However, in final product manufacturing, the **surface-mount technique** (SMT) became more widespread. Sometimes it is necessary or easier to use **surface-mount devices** (components in SMT-dedicated casings, SMD) already at the prototyping stage. For this purpose, special universal PCBs are manufactured that enable soldering an SMD and providing one or more mounting holes per each of its pins. Using these holes and the through-hole technique, a complete circuit prototype can be assembled. Such boards usually do not have metal traces except for those connecting device pins with corresponding mounting holes.

### 2.1.b. Circuit design

As the universal PCB used in this exercise has a pre-manufactured trace layout, circuit design activities are limited to:

- 1) planning the device placement,
- 2) determining if and where additional connections are needed.

Action 2 is usually necessary as a universal PCB obviously is 'universal' only to some extent. Before starting the PCB design. The additional connections are realised in one of the following ways:

- 1) with an ordinary insulated conductor—usually on the component side; both connector ends are passed through mounting holes and soldered to the solder pads just as device leads are;
- 2) with a bare wire, e.g. dedicated silvered copper wire or simply a component lead fragment cut off—usually on the device side (if on the solder side, it is necessary to ensure that the wire does not cause unwanted shorts along its length, also when incidentally deformed); wire mounting is done as previously;
- 3) with solder on the solder side (only possible when neighbouring traces are to be connected)—in this case solder pads are usually not occupied;
- 4) with a longer lead of an element connected to the same voltage as the points being connected (only possible if such a lead exists), bent on the solder side in line with the designed connection— this is a more reliable and easier alternative

to technique 3 as the laminate is often covered with a solder resist layer counteracting solder connecting neighbouring pads.

During universal PCB design the following rules are usually applied.

1. The design process is started with integrated circuit sockets. They are placed in dedicated areas, e.g. in the case of the board shown in Fig. 2 pins would be placed apart at both sides of the double horizontal traces. On larger boards, integrated circuits are usually placed in the middle.
2. Integrated circuits impose particular long traces to be chosen as supply and ground. Usually, supply and ground pins are top left and top right, or top left and bottom left, or top left and bottom right ones—this must be checked in the data sheet. It is desirable that a maximum number of devices are directly connected to a supply (or ground) trace.
3. If the PCB has special solder pads for specific connectors, placement begins with these connectors and then integrated circuits connected to them are placed.
4. After the integrated circuits, other devices are placed. One should start with those devices that are closest (in the electrical schematic or according to functional requirements) to the integrated circuits. De-coupling capacitors are placed first.
5. When placing passive elements, the designer should take advantage of the possibility of shorting or—the opposite—leaving long device leads. Vertical mount and appropriate shorting of the leads of an axial case enables inserting them even in neighbouring holes. On the other hand, making use of their full (or slightly shortened) length may eliminate the need for additional connections.
6. It should be kept in mind that device cases have determinate geometrical dimensions. They may cover up and make inaccessible some neighbouring mounting holes. This especially concerns electrolytic capacitors, coils, larger diodes and transistors, diode bridges, buttons, potentiometers and connectors.
7. Device terminals that are mutually connected in the electrical schematic should be placed on one conducting trace. Only when this is impossible, an additional connection is made.
8. Two solder pads should be provided for each additional connection. When neighbouring traces are to be connected, this may be done using solder itself (and possibly an additional supporting wire) on the solder side, without occupying any mounting holes, as described above.
9. No loops should be created together with the additional connections, i.e. moving along traces and additional connections in a chosen direction, we should never get back to the starting point. Loops will behave as antennas, emitting and intercepting electro-magnetic disturbances which may cause improper circuit operation.
10. If coils are present in the circuit (not the case of the present exercise), it should be avoided to place them in the vicinity of integrated circuits or above traces connected to any other devices.
11. Power loops (high-voltage or high-current ones) should have the shortest perimeter and the lowest area enclosed possible. Their elements should therefore be placed the closest possible one to another.
12. Additional connections in high-current loops are realised using high-cross-section wires. Due to the low diameter of mounting holes, it may be necessary to solder these wires on the solder side.
13. Also the leads of high-current devices may have a diameter larger than the diameter of mounting holes. This should be checked on the board design stage (in device data sheets) or after devices are collected (empirically) but *before* circuit assembly starts. Too tight holes will have to be broadened using a drill, taking special care not to damage the solder pads and adjacent traces.

14. Device placement is usually finalised with connectors and potentiometers, which must be put in easily accessible points. These frequently are the board edges. Connection paths to the rest of the circuit should be the shortest possible and should involve the least possible number of additional connections.
15. In the case of prototypes, additional horizontal shorts, vertical measurement pins or measurement points (small loops) are mounted on the board. There are intended to enable attaching oscilloscope probes to the key circuit nodes during testing.

## 2.2. Using the worksheet and design example

### 2.2.a. Design support worksheet

In order to limit the number of errors and to ease design verification, you should use the worksheet *plytka\_uniwersalna.ods* if designing with the prototype board. A general description of this worksheet is available as an attachment to this manual.

Now we will follow an exemplary design based on a universal PCB. Let's assume that the circuit shown in Fig. 3 has to be assembled and that the universal prototyping board already presented in Fig. 2 is to be used.

### 2.2.b. Circuit for the design example

The exemplary circuit has a supply input through the Z<sub>1</sub> connector (a terminal block) and a double signal input through the Z<sub>2</sub> connector. The supply is stabilised with the C<sub>1</sub> electrolytic capacitor. High-frequency disturbances are carried off to the ground through the C<sub>2</sub> de-coupling ceramic capacitor.

The U<sub>1</sub> integrated circuit includes 4 NAND gates numbered from 1 to 4 whose inputs are labelled as A and B, and outputs as Y. The VCC pin is the supply positive potential and the GND pin is the supply ground. These gates are used as buffers for signals 1 and 2 that come from some outputs with too low a current capability to make the Light Emitting Diodes (LEDs) light up. In the case of the signal 1 it is an inverting buffer as a single NAND gate with shorted inputs acts as a NOT gate. For the signal 2 it is a non-inverting buffer as two such NOT gates are connected in cascade.

Gate outputs are supplied from a voltage connected to the VCC and GND pins, so from the source connected to the circuit through the Z<sub>1</sub> connector. We assume that current capability of this source is sufficient to light up the LEDs. Setting a given Y output in the logical zero state, i.e. the low level, means electrically connecting this output to the GND pin, so the ground. In the case of 1Y and 4Y outputs this will close a loop starting from Z<sub>1</sub> connector's terminal 1 and ending at its terminal 2: through D<sub>1</sub> and R<sub>1</sub> or through D<sub>2</sub> and R<sub>2</sub> components. This will enable current flow and lighting up the corresponding LED.

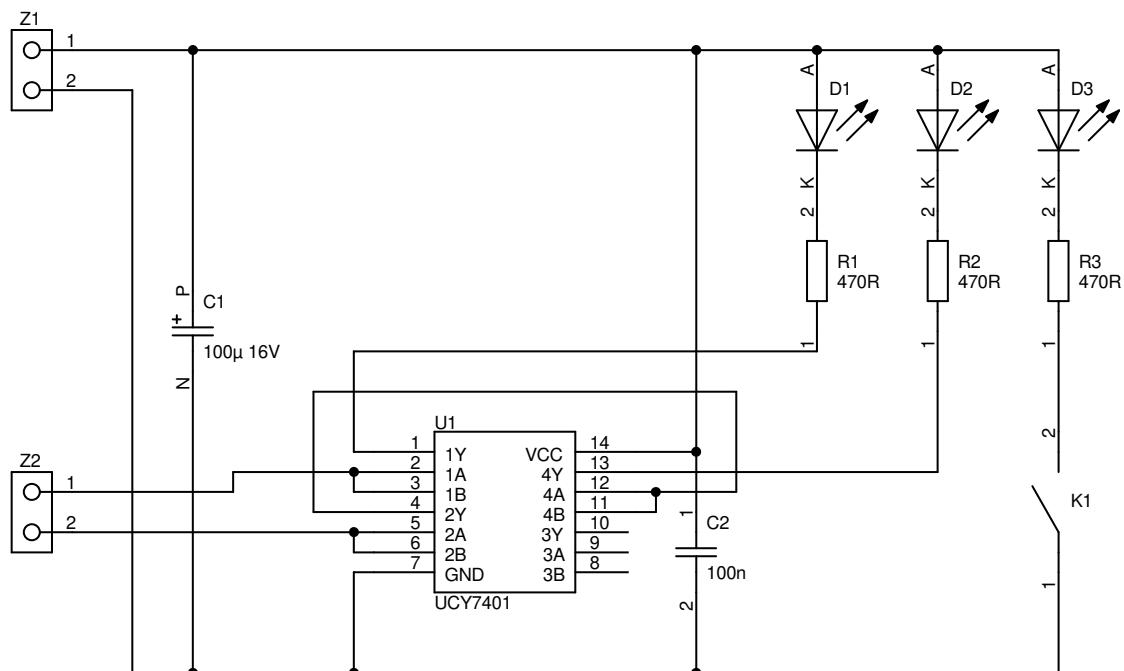


Fig. 3. Schematic of the circuit used in the design example



The third LED (D<sub>3</sub>) is supplied directly and turns on when the K<sub>1</sub> button is pushed (or the key is closed). The 3 resistors R<sub>1</sub>, R<sub>2</sub> and R<sub>3</sub> enable setting the diode current value, which is equal to the supply voltage decreased by the voltage drop across the diode and divided by the resistor's value.

**2.2.c. Preparation for design**

In order to start the design, it is necessary to know the lead arrangement and spacing for the particular components as well as their case dimensions (precisely, the dimensions of case projection onto the board surface). Together with professional PCB design software, case outline libraries are delivered. In our case, outlines and lead arrangement are shown in Table 1 against the solder pads grid of the board to be used (so, a single distance between holes is 2.5 mm).

The universal board together with all the components are pictured in Fig. 4.

Table 1. Lead arrangement and case outline for the components used in the design example (terminal labels are consistent with Fig. 3)

Component	Integrated circuit, DIP-14	Miniature button
Case outline with lead arrangement		
Component	Terminal block, 2-pole, RM 5	Electrolytic capacitor, vertical, Ø6, RM 2,5
Case outline with lead arrangement		
Component	Light Emitting Diode	Capacitor, ceramic disc
Case outline with lead arrangement		
Component	Resistor, 1/4 W, horizontal mount	Resistor, 1/4 W, vertical mount
Case outline with lead arrangement		

Design begins with the entry of the solder pads and connecting traces image to the spreadsheet *Płytki*, the effect being presented in Fig. 5. Grey represents the laminate surface, white represents metallic paths (traces) and black frames represent solder pads (so, mounting holes as well).

Into the spreadsheet *Węzły schematu* data about electrical connections in the circuit according to Fig. 3 are introduced. The considered circuit has 11 electrical nodes which results in the below circuit description.

- Z1.1 C1.P U1.14 C2.1 D1.A D2.A D3.A
- Z1.2 C1.N U1.7 C2.2 K1.1
- Z2.1 U1.2 U1.3
- Z2.2 U1.5 U1.6
- U1.4 U1.11 U1.12
- U1.1 R1.1



R1.2 D1.K  
 U1.13 R2.1  
 R2.2 D2.K  
 K1.2 R3.1  
 R3.2 D3.K

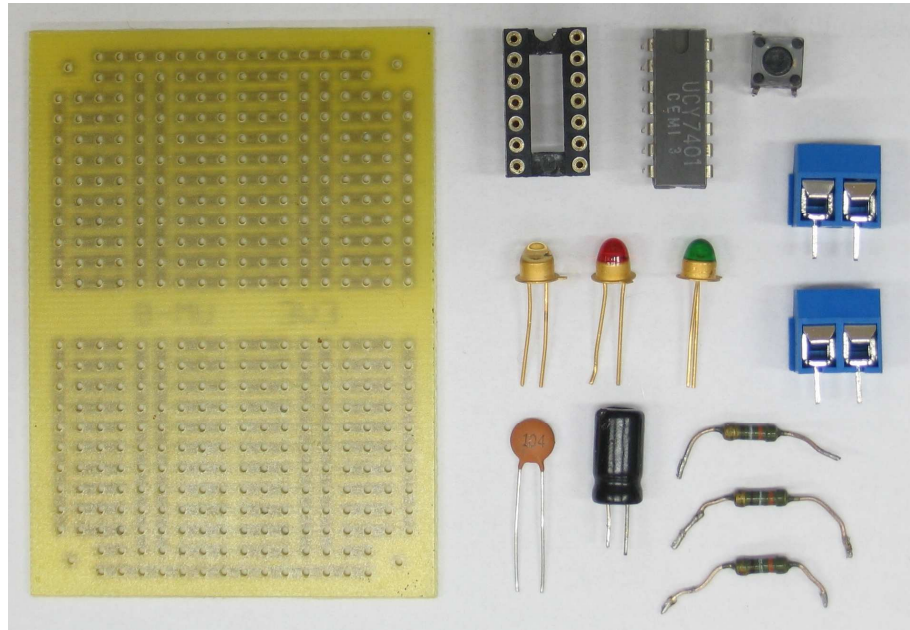


Fig. 4. Board and components for the design example

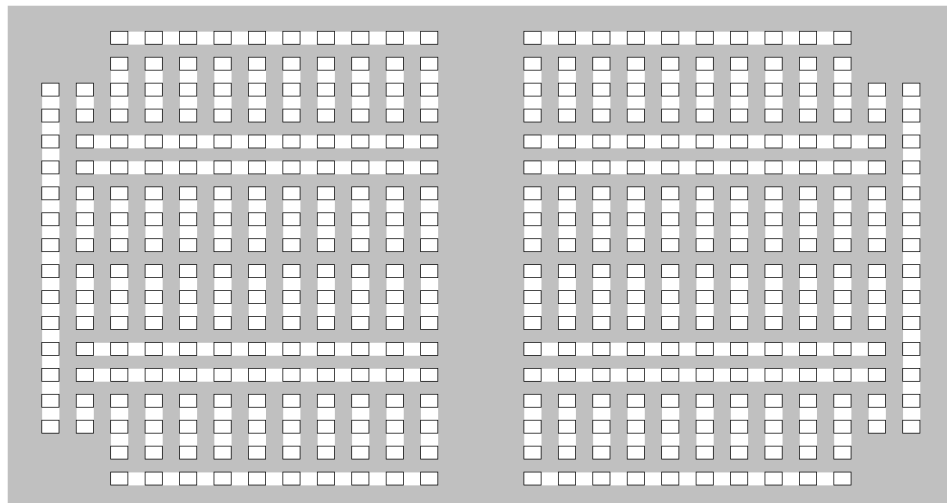


Fig. 5. Solder pads and pre-manufactured connections image defined in the spreadsheet Płytki

### 2.2.d. Component placement and connection planning

We are now beginning the design process proper.

1. We start with the  $U_1$  integrated circuit (see Section 2.1.b, pt 1. We will place it along one of the long horizontal traces. As it has two input signals connected from the left-hand side (in the schematic) and the  $Z_1$  terminal block has fairly large dimensions, we decide to locate the IC in the bottom left quarter of the board, so that there is enough space for the terminal block above it (on the board). On the other hand, right of the IC (on the board) we leave free space for the  $C_2$  de-coupling capacitor. The result is shown in Fig. 6(a).

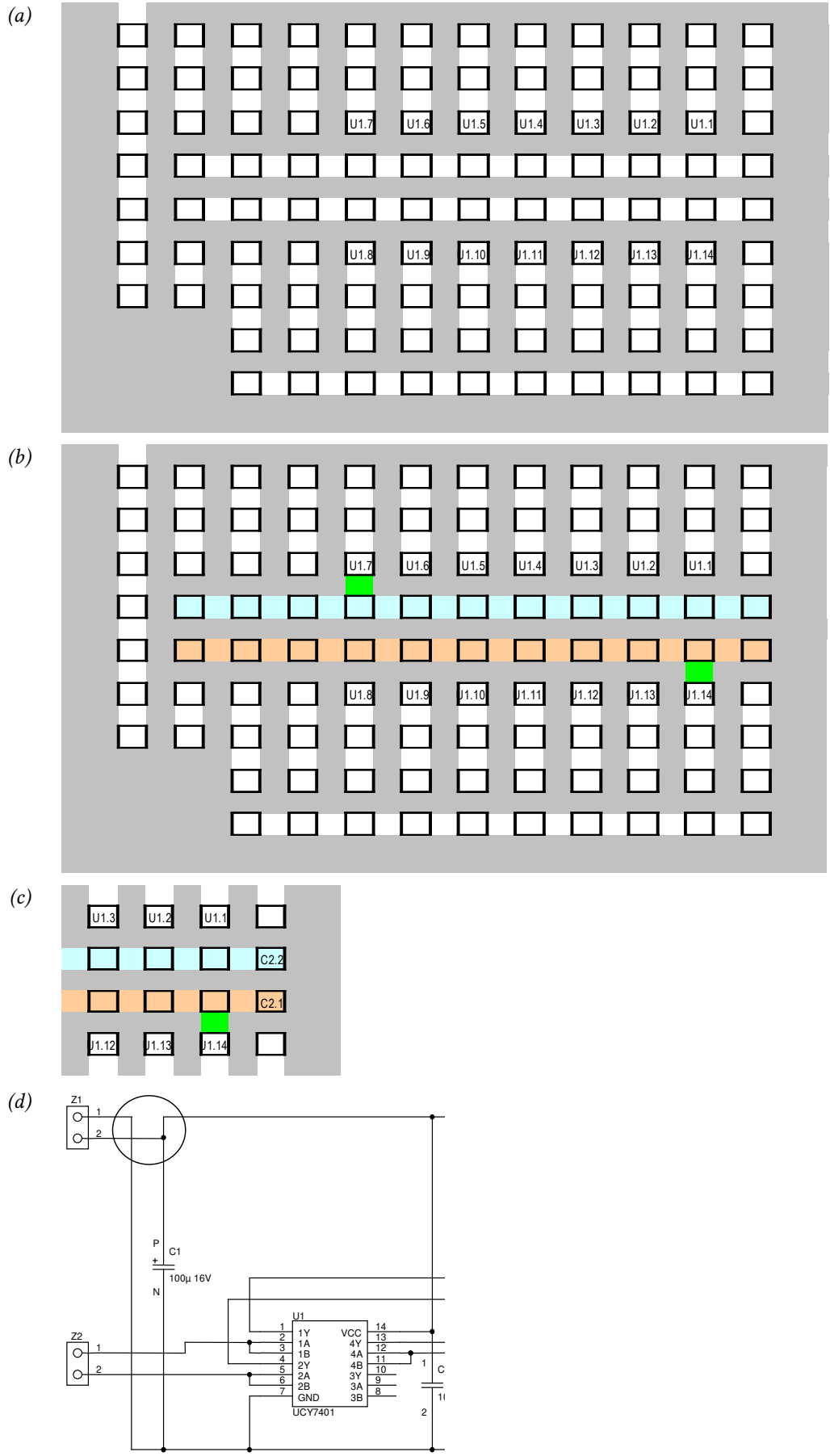


Fig. 6. Board design process

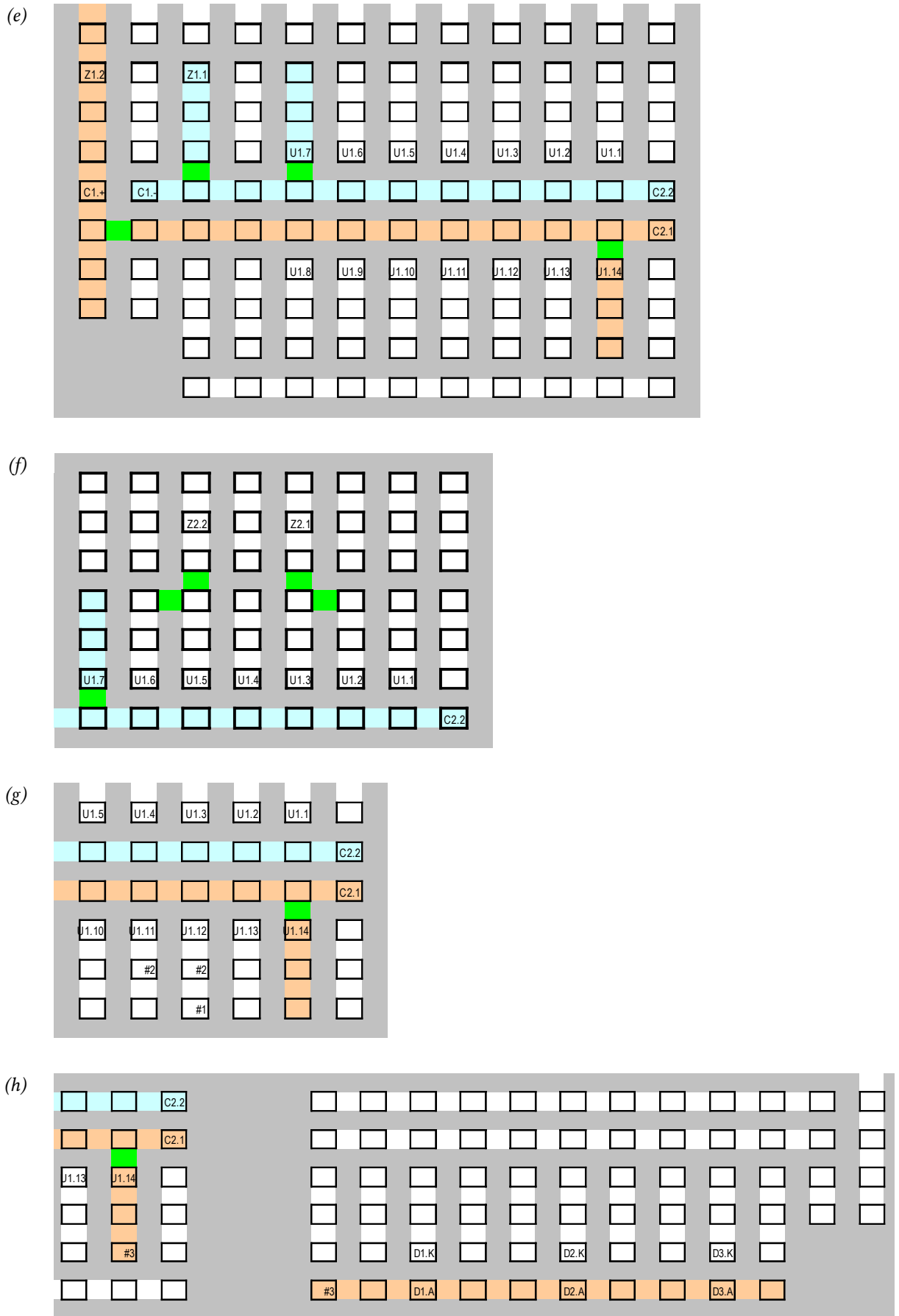


Fig. 6 (cont.) Board design process

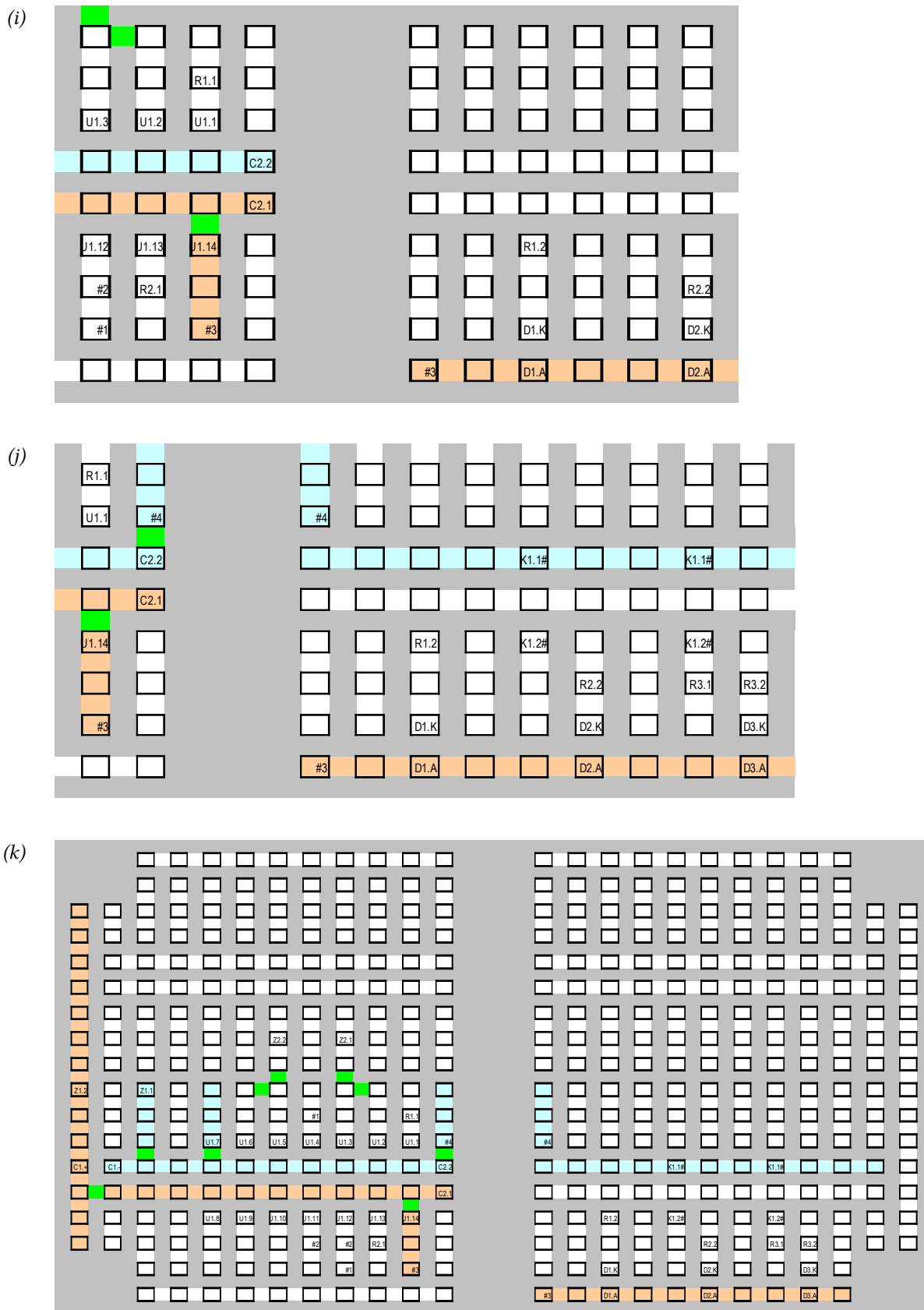


Fig. 6 (cont.) Board design process

2. The IC imposes specific long horizontal traces to be chosen as supply (the one neighbouring the pin 14 or VCC, see Section 2.1.b, pt 2) and as ground (the one neighbouring the pin 7 or GND). We mark them with pink and cyan and connect to the appropriate pins of the U<sub>1</sub> integrated

circuit using solder on the solder side (a wire can be avoided as neighbouring traces are being connected, see Section 2.1.b, pt 8), which we mark with green. The result is shown in Fig. 6(b).

3. The  $C_2$  de-coupling capacitor is inserted between the supply and ground traces, the closest possible to the supply pin (VCC) of the  $U_1$  IC (see Section 2.1.b, pt 4), taking care to connect terminal 2 to the ground and terminal 1 to the supply. Otherwise, the automated design check will fail because the board will be incompatible with the schematic. The result is presented in Fig. 6(c).
4. On the left end of the supply traces there is enough space for connecting the supply (the  $Z_1$  terminal block) and the  $C_1$  blocking capacitor. It is best to insert the capacitor directly into the traces as there will so be no need for any additional connections; in this case, we will place the terminal block above the capacitor. The supply path has therefore to be bent to the top (towards the terminal block), for which purpose we use the long vertical trace along the board's edge. The ground trace will be bent along the shorter path. We plan to make all the necessary connections using solder on the solder side. We update supply and ground path colouring and check whether they do not form a loop (see Section 2.1.b, pt 9).

If the terminal block was to be inserted according to the schematic, i.e. with the ground connected to  $Z1.2$ , the front of this block would have to face the  $C_1$  capacitor, which would impede inserting wires (see Section 2.1.b, pt 14). We therefore insert it with its *back* facing the capacitor which forces us to modify the electrical schematic by connecting the ground to  $Z1.1$  and the supply to  $Z1.2$  [see Fig. 6(d) where a circle shows the modified part]. The final result is presented in Fig. 6(e).

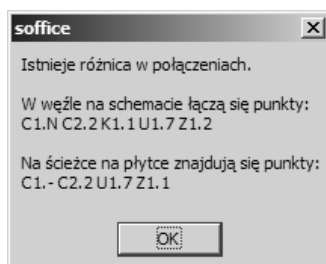
5. Now we can place the  $Z_2$  terminal block, however, making sure to leave enough space between it and the IC to make the connections going out from pins 1 and 4. We can notice that it will be profitable to locate the  $Z2.1$  pin just opposite the  $U1.3$  pin, and  $Z2.2$  opposite  $U1.5$  because such connections are present in the electrical schematic. We short the pins as appropriate,  $U1.2$  with  $U1.3$  and  $U1.5$  with  $U1.6$ , using solder as they are placed on neighbouring traces. The result is presented in Fig. 6(f).
6. We make last connections in the vicinity of the IC:  $U1.4$  with  $U1.12$  using a wire that we label #1 and  $U1.12$  with  $U1.11$  using a wire that we label #2. The result is presented in Fig. 6(g).
7. Only diodes and resistors are left for placement now (except for the  $K_1$  button that we will keep aside until the location of  $R_3$  and  $D_3$  components connected with it is determined). As all the three anodes must be at the supply potential, we will connect them to one of the long traces (see Section 2.1.b, pt 7). We choose the one running along the edge of the bottom right quarter of the board because it is located relatively close to the IC and there is enough space above it for the three resistors and the button. The supply is brought to this trace from pin 14 of the IC using the wire #3. We should keep in mind that according to the table, each diode occupies about 3 solder pad distances (see Section 2.1.b, pt 6). The result is presented in Fig. 6(h).
8. The leads of  $R_1$  and  $R_2$  resistors are originally longer than the minimum lengths shown in Table 1. We can take advantage of this to make direct connections between the cathodes of  $D_1$  and  $D_2$  and the corresponding outputs of the IC, without using any additional wires (see Section 2.1.b, pt 5). We must only try to avoid their crossing with other components or provide an appropriate (vertical) distance between them, or protect the leads with insulating tubes. The result is presented in Fig. 6(i).
9. On the contrary, the  $R_3$  resistor will be mounted vertically, to fit the  $K_1$  button just beside. The button will be placed in such a way that its other end is inserted into the long horizontal line. We continue along this line to the left, to a point nearest the existing ground trace, and we insert the wire #4 for the missing part of the connection. Due to the closest solder pad being occupied by the  $C2.2$  terminal, we insert the other end of the wire do the neighbouring, free pad and connect to the ground trace using the solder.

Attention should be paid to terminate the labels of the  $K_1$  button's terminals with the hash sign “#” as they are shorted in pairs inside the component. In order for this to be taken into account during design check, both terminals of a pair must be given the same label which moreover must end with a hash sign (see the worksheet description attached).

10. Component placement is finished. The result is presented in Fig. 6(k).

### 2.2.e. Design verification and improvement

11. We will now check the correctness of our design using the macro *\_SprawdzPolaczenia*. Verification causes an error message to be displayed telling us about discrepancy in connections between the schematic and the board:



In the 3<sup>rd</sup> line of such a message, terminals connected to a same node in the schematic are listed. In the 5<sup>th</sup> line, terminals connected to the same node on the board are listed. We can state that there are 3 differences between these lists:

- 1) there is a C1.- terminal on the board which, according to the schematic, should be labelled C1.N; on this occasion, C1.+ should obviously be also changed to C1.P;
- 2) the K1.1 terminal is not present in the board-based list which means we have not connected it to the ground; indeed, we have mistakenly placed the second end of the wire #4, opposite the first one instead of one solder pad below; we move it to the proper location;
- 3) the trace corresponding to the displayed list connects to Z1.1 while based on the schematic it appears that it should connect to Z1.2; in this case, this is the sheet *Węzły schematu* that is wrong as we forgot to update it after the connections of the Z<sub>1</sub> connector were exchanged.

After correcting, the schematic is described as follows:

```
Z1.1  C1.N  U1.7  C2.2  K1.1
Z1.2  C1.P  U1.14 C2.1  D1.A  D2.A  D3.A
Z2.1  U1.2  U1.3
Z2.2  U1.5  U1.6
U1.4  U1.11 U1.12
U1.1  R1.1
R1.2  D1.K
U1.13 R2.1
R2.2  D2.K
K1.2  R3.1
R3.2  D3.K
```

while the new image of the board is presented in Fig. 8.

12. We launch the check again. This time the error concerns the following terminals:

```
Schemat:  U1.11 U1.12 U1.4
Płytką:   U1.10
```

where *Schemat* lists the terminals in the schematic and *Płytką* lists the terminals on the board.

We check the unconnected U1.10 terminal which appears in the board-based list and we state that it indeed should be floating. The same applies to U1.9 and U1.8. Unfortunately, we did not allow for it in the node list. We must therefore introduce three additional nodes to the sheet *Węzły schematu*, with only one terminal assigned to each of them. Sheet contents are now as follows:

```
Z1.1  C1.N  U1.7  C2.2  K1.1
Z1.2  C1.P  U1.14 C2.1  D1.A  D2.A  D3.A
Z2.1  U1.2  U1.3
Z2.2  U1.5  U1.6
```

U1.4    U1.11   U1.12  
U1.1    R1.1  
R1.2    D1.K  
U1.13   R2.1  
R2.2    D2.K  
K1.2    R3.1  
R3.2    D3.K  
U1.8  
U1.9  
U1.10

13. We launch the check again. There is no error now which means that the connections planned on the board are consistent with those described in the sheet *Węzły schematu* that reflects the electrical schematic.

Fig. 7 shows the circuit assembled according to Fig. 8 and operating. The original circuit may be inspected in the laboratory room as is also the case of an exemplary dimmer as designed in the present exercise.

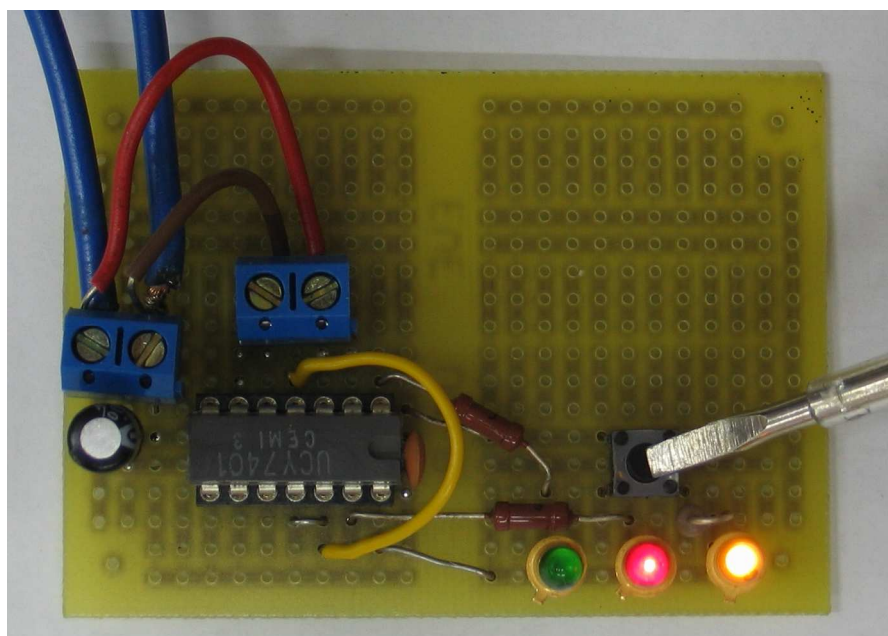


Fig. 7. The example circuit assembled and operating



Fig. 8. Final image of the universal board obtained in the design example



## Exercise Introduction

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### 3. Exercise Aim and Plan

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The aim of this exercise is to get acquainted with the principal issues in design and prototyping of switch-mode power electronic circuits. A buck DC converter will be the object of a design assignment, where a MOSFET and a Schottky diode will be applied.

This design assignment will be realised according to the engineer's work flow diagram presented in Fig. 9 with the exception that:

- the idea of the circuit (item 1) is known beforehand;
- component parameters will be used as measured by their manufacturers and indicated in their technical documentation (item 4);
- ready-made universal simplified component models (item 5) will be used.

This exercise will make it possible to become acquainted with the basics of control circuit design for power semiconductor devices based on the principle of variable pulse width. Additionally, you will get acquainted with circuit design rules using universal PCBs, electronic circuit assembly (through-hole) and the procedures of their commissioning and testing.

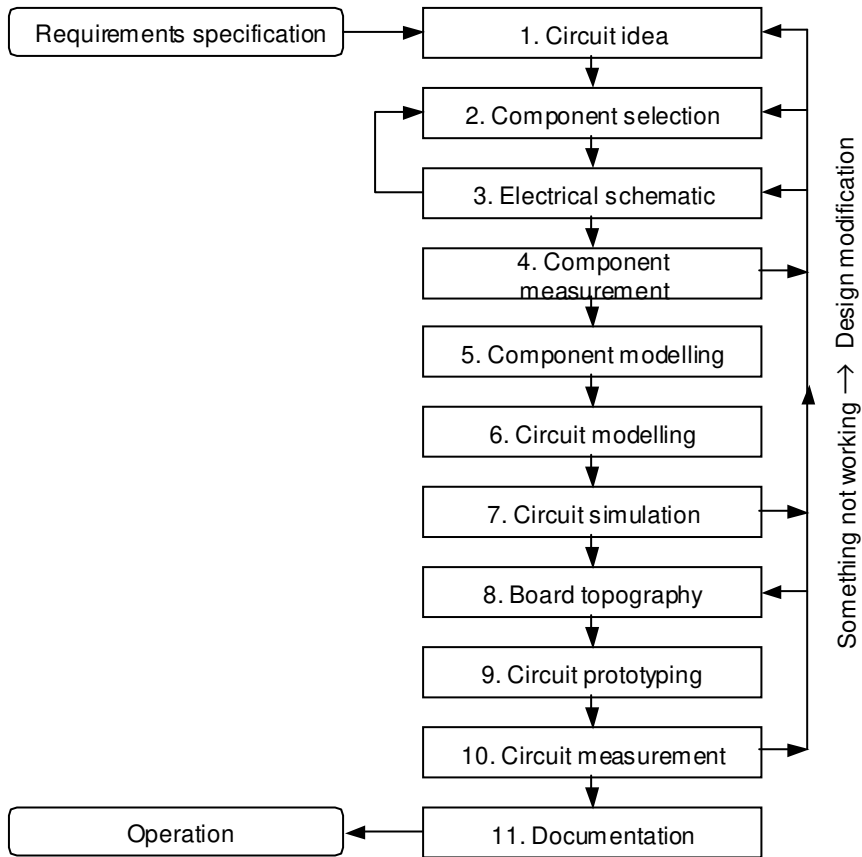


Fig. 9. Work flow diagram of a circuit design and prototyping engineer

## 4. DC/DC Converters

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### 4.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
A	Ben	4.5	4.1.a–b		

Additionally, from Manual 0 references:

0 B	Eri	1.1	4.1.b, 4.2a–b, 4.3.a,c,d, 5.1.a–b		
0 E	Ras	6.2	4.2, 4.3.a–c		4.2

### 4.2. Switch-mode control

Obtaining the switch-mode operation of a converter circuit requires switch-mode control of semiconductor devices instead of continuous (linear) control. A controlling quantity  $x$  (current or voltage) then takes the form of a pulse wave. It consists of periodically repeated pulses, i.e. sections of a level higher than the idle one, whose shape, to simplify, can be considered rectangular [see Fig. 10(a)].

A pulse wave is described by the following parameters:

- (1) **period of repetition**  $T_p$  which is of course the shortest time after which the waveform repeats, so e.g. the interval between the beginnings of successive pulses;
- (2) **frequency of repetition**  $f_p$  which is the inverse of the period of repetition

$$f_p = \frac{1}{T_p} \tag{4.1}$$

- (3) **pulse width**  $t_p$  which is the duration of the top of the pulse;
- (4) **duty cycle** (also called *duty ratio*)  $D$  which is the ratio of the pulse width of the period of repetition:

$$D = \frac{t_p}{T_p} \tag{4.2}$$

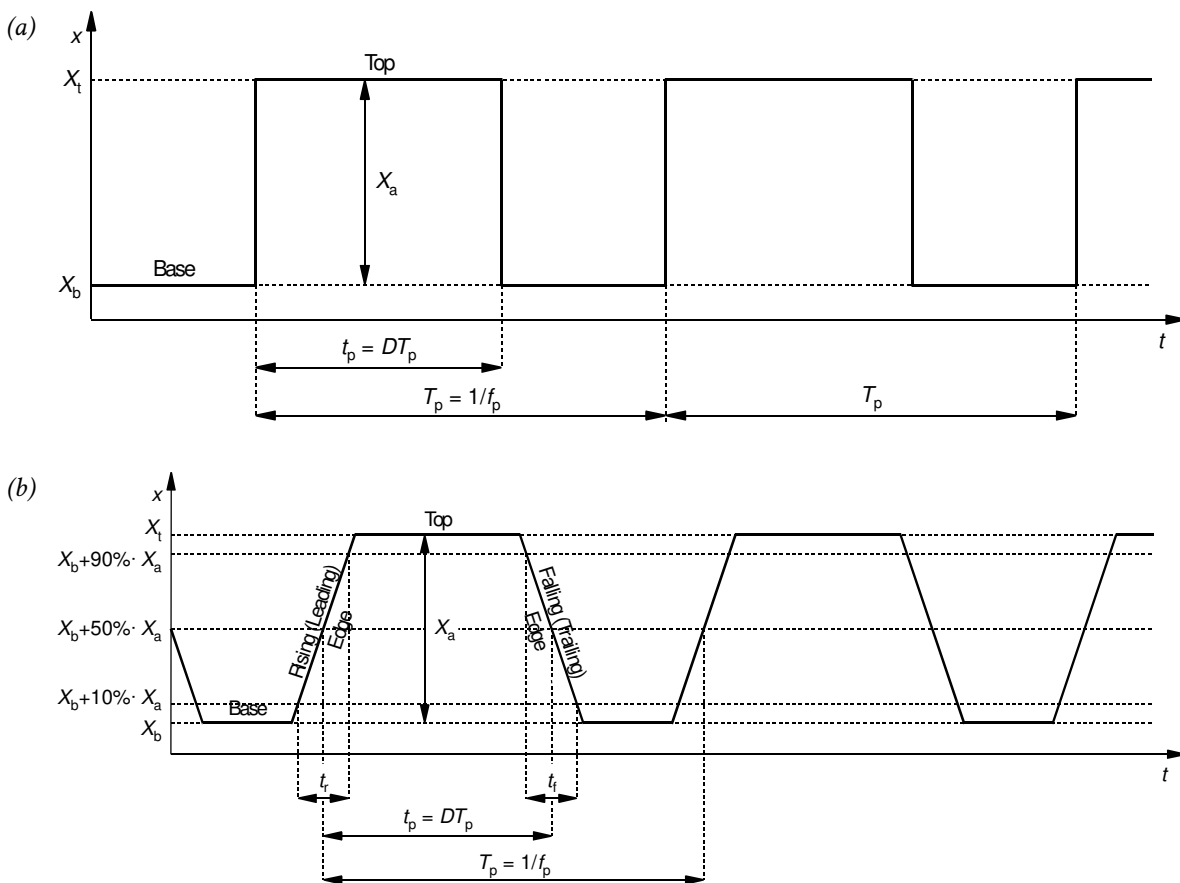


Fig. 10. Pulse wave and its basic parameters: (a) the ideal waveform; (b) a waveform with finite edge steepness

As it can be easily seen, just one of the parameters 1 or 2 and one of the parameters 3 or 4 are sufficient for an unambiguous description of a pulse wave in the time domain.

In the domain of the given electrical quantity (current or voltage), a pulse wave is described by:

- (5) **low level**  $X_L$  which is the value of  $x$  corresponding to the base of the pulse;
- (6) **high level**  $X_H$  which is the value of  $x$  corresponding to the top of the pulse;
- (7) **amplitude**  $X_m$  which is the distance between the low and the high levels

$$X_m = X_H - X_L \quad (4.3)$$

As it can be seen, any two of the parameters 5 to 7 are sufficient for an unambiguous description of a pulse wave.

In power electronics, very often waveforms with a zero base level ( $X_L = 0$ ) are met, for which  $X_H = X_m$ . Because of the prevalence of this case and due to the considerable simplification of relationships that are obtained, it is usually the zero base level that is assumed in analysis.

The above mentioned parameters fully describe only ideal pulses. In power electronics, it is the non-zero edge duration that is the most often considered feature of a real pulse wave. These edges are described by [see Fig. 10(b)]:

- (8) **rise time**  $t_r$ , i.e. the time it takes for the waveform to rise from 10% to 90% of its amplitude, which is a measure of the duration of the rising edge (also called the leading edge);
- (9) **fall time**  $t_f$ , i.e. the time it takes for the waveform to fall from 90% to 10% of its amplitude, which is a measure of the duration of the falling edge (also called the trailing edge).

Other nonidealities (e.g. overshoots, settling time, jitter) usually do not affect the macroscopic operation of model (academic, ideal) converters. We will therefore neglect them. However, taking them into account becomes necessary at the optimization stage of physical (real) circuits where they can cause undesirable microscopic phenomena adversely affecting the overall system operation.



## 5. Buck Converter

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### 5.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
B	Eri	2.1, 2.2, 2.5	4.3.a,b,d, 5.1.a–b, 5.2.a–b, 5.3		5.3
C	Eri	4, 4.1.1, 4.1.5	5.1.c, 5.2.c		
			5.1.c–f		5.2
			5.4		5.4
			5.5		5.5

## 5.2. Buck converter passive components

### 5.2.a. Obtaining a continuous current flow with an inductor

The role of the two passive components of the buck DC/DC converter—the inductor (choke) and capacitor—may be analysed from the signal point of view (low-pass filtering) but also from the power transmission point of view. Most receivers (e.g., microprocessors) require constant power supply. A buck converter without an LC filter is called ‘voltage chopper’ because its input voltage appears at the receiver as ‘chopped’. Power flow is therefore temporarily and periodically interrupted.

Wired power transmission necessitates charge motion in a conductor, or current. Thus, constant power delivery necessitates uninterrupted current flow. To obtain it, a component should be inserted into the circuit that will prevent the output current from immediately dropping down to zero in the moment of switch opening. The inductor is well known for this property which follows from energy conservation principle. It says that any change in energy of a system (in this case, the inductor) may only result from additional energy being delivered from outside. No energy can be delivered in zero time as this would necessitate infinite instantaneous power

$$p = \frac{dW}{dt} \quad (5.1)$$

which is unrealistic. Thus, neither can inductor’s energy change abruptly. This energy  $W_L$  is accumulated in magnetic field caused by the current  $i_L$  flowing through the inductor; they are related to each other by

$$W_L = \frac{Li_L^2}{2} \quad (5.2)$$

where  $L$  is the inductance of the inductor. Therefore, the current through an inductor cannot change abruptly.

In order to make current through the receiver (load) continuous, the inductor must be inserted so as the receiver current  $i$  flows through it, thus in series. This is shown in Fig. 11(a).

### 5.2.b. Analytical description of the inductor’s operation

In each of the two sub-intervals of the switching period, the inductor is found in a series RL circuit which is described with Kirchhoff’s voltage law

$$E = v_L + v \quad (5.3)$$

where  $v_L$  is the voltage across the inductor and  $E$  is an effective forced voltage which is  $V_g$  in sub-interval 1 (Fig. 12a) and 0 in sub-interval 2 (short-circuit which is equivalent to zero voltage source, Fig. 12b). Using Ohm’s law and inductor equation and taking into account that  $i = i_L$  in both subintervals, we obtain the equation of the RL circuit

$$Ri + L \frac{di}{dt} - E = 0 \quad (5.4)$$

Using any method of differential equation solution, the solution is found to be

$$i(t) = i(t_0) + \left( \frac{E}{R} - i(t_0) \right) \cdot \left( 1 - e^{-\frac{t-t_0}{\tau}} \right) \quad (5.5)$$



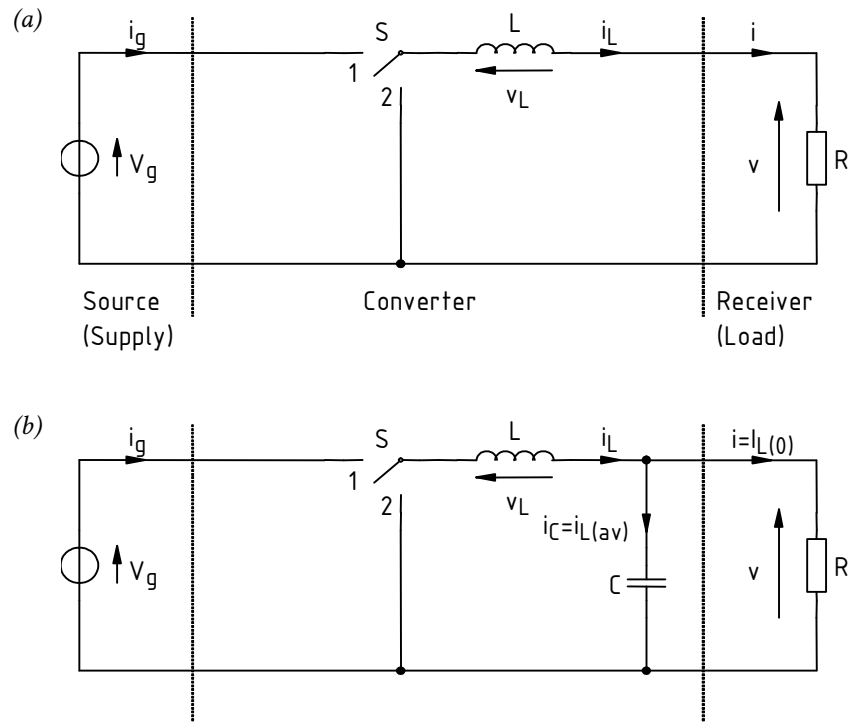


Fig. 11. Buck converter circuit: (a) with only the inductor; (b) with the capacitor added

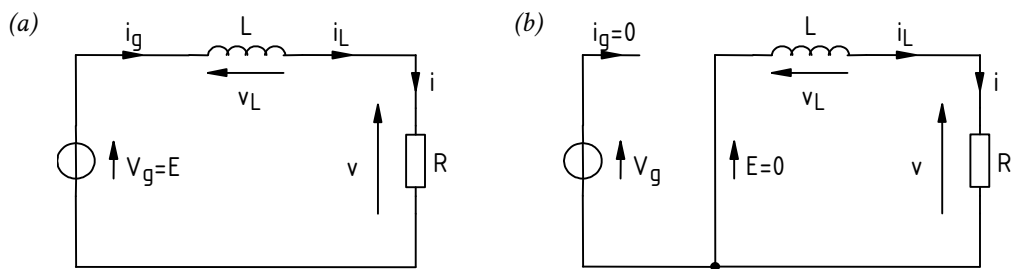


Fig. 12. Reduced circuit topology of Fig. 11(a): (a) during sub-interval 1; (b) during sub-interval 2

where  $\tau$  is called the time constant and equals

$$\tau = \frac{L}{R} \tag{5.6}$$

and  $t_0$  denotes the beginning of a given sub-interval. Let us apply Eq. (5.5) to either sub-interval.

1. For sub-interval 1,  $t_0 = t_1$ . Assume that the current is zero initially:  $i(t_0) = 0$ . Then,

$$i(t) = \frac{V_g}{R} \cdot \left( 1 - e^{-\frac{t-t_1}{\tau}} \right) \tag{5.7}$$

Substituting  $t = t_1$  and  $t = \infty$  we have

$$i(t_1) = \frac{V_g}{R} \cdot \left( 1 - e^{-\frac{t_1-t_1}{\tau}} \right) = \frac{V_g}{R} \cdot (1 - e^0) = \frac{V_g}{R} \cdot (1 - 1) = 0 \tag{5.8}$$

which complies with our assumption, and

$$\begin{aligned}
 i(\infty) &= \frac{V_g}{R} \cdot \left(1 - e^{-\frac{\infty-t_1}{\tau}}\right) = \frac{V_g}{R} \cdot (1 - e^{-\infty}) = \frac{V_g}{R} \cdot \left(1 - \frac{1}{e^\infty}\right) = \frac{V_g}{R} \cdot \left(1 - \frac{1}{\infty}\right) = \\
 &= \frac{V_g}{R} \cdot (1 - 0) = \frac{V_g}{R}
 \end{aligned}
 \tag{5.9}$$

The current therefore changes exponentially, rising from 0 up to  $V_g/R$ . This has been illustrated in Fig. 13(a).

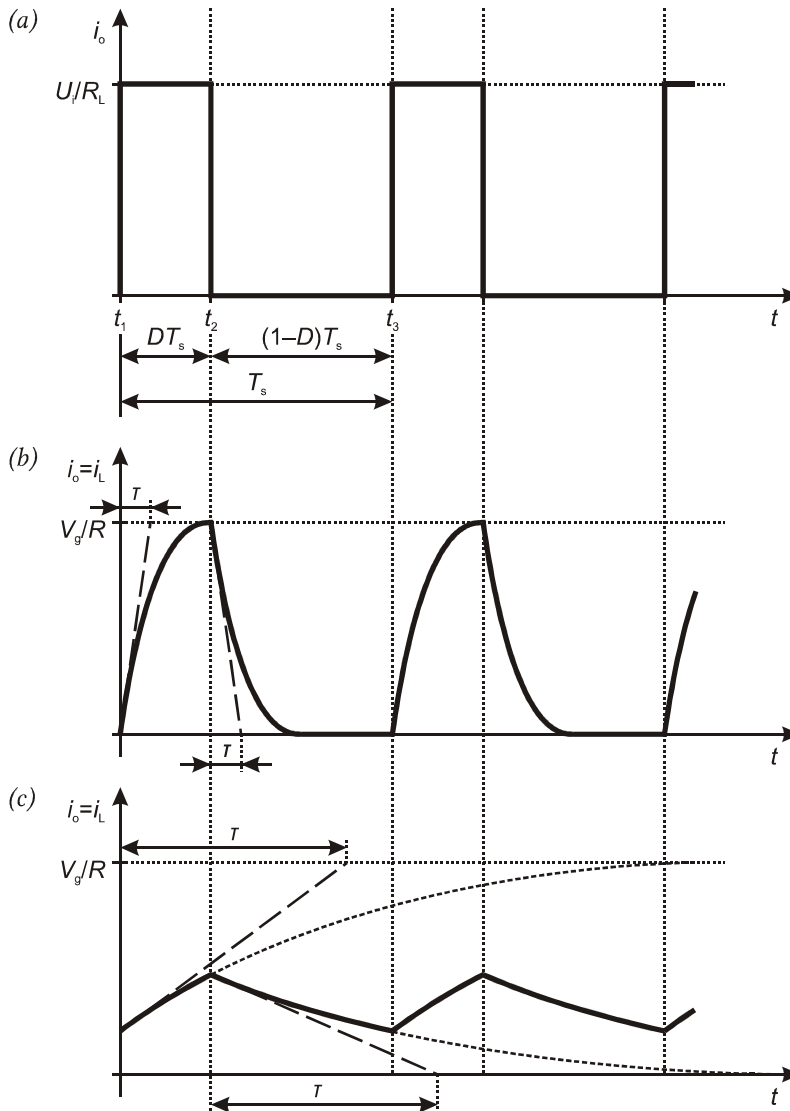


Fig. 13. Output current waveform: (a) without an inductor; (b) with an inductor (Fig. 11a) of small inductance ( $\tau \ll T_s$ ); (c) with an inductor if large inductance ( $\tau \approx T_s$ )

- At the beginning of sub-interval 2 ( $t_0 = t_2$ ), the current equals that at the end of sub-interval 1. We therefore obtain

$$i(t) = \frac{V_g}{R} - \frac{V_g}{R} \cdot \left(1 - e^{-\frac{t-t_2}{\tau}}\right) = \frac{V_g}{R} \cdot \left(1 - 1 + e^{-\frac{t-t_2}{\tau}}\right) = \frac{V_g}{R} \cdot e^{-\frac{t-t_2}{\tau}}
 \tag{5.10}$$

Substituting  $t = t_2$  and  $t = \infty$  we have

$$i(t_2) = \frac{V_g}{R} \cdot e^{-\frac{t_2 - t_1}{\tau}} = \frac{V_g}{R} \cdot e^{-0} = \frac{V_g}{R} \cdot 1 = \frac{V_g}{R} \quad (5.11)$$

which complies with our assumption, and

$$i(\infty) = \frac{V_g}{R} \cdot e^{-\frac{\infty - t_1}{\tau}} = \frac{V_g}{R} \cdot e^{-\infty} = \frac{V_g}{R} \cdot 0 = 0 \quad (5.12)$$

The current therefore changes exponentially, falling from  $V_g/R$  down to 0. This has been illustrated in Fig. 13(b).

The time of current settling down depends on the time constant  $\tau$ . It can be calculated that its steady-state value is reached with an accuracy of 1% (0,01) after a time equal  $\tau \ln(1/0,01) \approx 4.6\tau$ . It therefore follows from (5.6) that the larger the inductance (for given  $R$ ), the slower the current rise and thus, the stronger the inductor opposes abrupt current changes. In power electronics, an inductor of an inductance large enough to visibly slow down current variation in time, is called a choke.

When choke inductance is sufficiently large, current is unable to attain the levels of  $V_g/R$  and 0 at the end of either sub-interval. This is demonstrated in Fig. 13(c). In general, a simplified condition for this occurring can be written down as

$$4\tau > T_s \quad (5.13)$$

where the number 4 results from rounding the value of 4.6 justified above. Substituting (5.6)

$$L > \frac{R}{4f_s} \quad (5.14)$$

As inductor current also flows through the load resistance  $R$ ,  $i$  current has the exact shape of  $i_L$ . According to Ohm's law, voltage  $v$  across the load resistance must also be of the same form.

### 5.2.c. Minimising voltage ripple using a capacitor

Using the inductor, we gained continuous output voltage, but it is still far from being constant. In most applications, minimising voltage ripple using only an inductor is impossible as it would result in unacceptable size, weight, cost and power loss. Moreover, an inductor is not capable of filtering high-frequency disturbance (short spikes and fast oscillations) that are inherently linked with switched-mode power converters.

For the above reasons, a second type passive component must be used: a capacitor. Its energy is expressed as

$$W_C = \frac{Cv_C^2}{2} \quad (5.15)$$

where  $C$  is the capacitor's capacitance and  $v_C$  is the voltage across it. It therefore follows from energy conservation principle that voltage across a capacitor cannot change abruptly.

In order to make use of this property, the capacitor must be inserted so that the receiver's voltage  $v$  appears across it. Only then it will slow down the variation of this voltage in time. This leads to the parallel connection shown in Fig. 11(b).

### 5.2.d. Analytical description of the capacitor's operation

After insertion of the capacitor, the inductor current  $i_L$  splits into two branches: the capacitor's one and the receiver's one. According to Kirchhoff's current law (cf. Fig. 11b),

$$i_L = i_C + i \quad (5.16)$$

The inductor current can be considered as the sum of a direct component  $I_{L(0)}$  and an alternating one  $i_{L(a)}$ :

$$i_L = I_{L(0)} + i_{L(a)} \quad (5.17)$$

where, based on Fourier analysis, the direct component is equal to the average value  $i_{L(av)}$  (level  $I$  in Fig. 2.10 of Ref. B). Consequently

$$i_{L(a)} = i_L - I_{L(0)} = i_L - i_{L(av)} \quad (5.18)$$

It is therefore the  $i_L$  waveform shifted down by its own average value. The  $i_{L(a)}$  waveform has therefore exactly the same shape but it is varying under and over the time axis (and not under and over the direct component level  $I$ ).

The magnitude of a capacitor's impedance is given by

$$|Z_C| = \frac{1}{\omega C} = \frac{1}{2\pi f C} \quad (5.19)$$

For  $f \rightarrow 0$  we have  $|Z_C| \rightarrow \infty$  which means that for the direct component, a capacitor presents a gap in the circuit. Thus, no direct component can ever flow through a capacitor. On the other hand, high frequency current components (such as the converter's switching frequency  $f_s$ ) will easily pass through as for  $f \rightarrow \infty$  we have  $|Z_C| \rightarrow 0$ .

It follows from (5.19) that the higher the capacitance  $C$ , the lower the impedance for a given frequency  $f$  will be. The capacitor  $C$  and the load resistance  $R$  form a current divider, whose action for a given frequency is described by the formulae

$$\begin{aligned} I_{C(f)} &= I_{L(f)} \frac{R}{|Z_C(f)| + R} = I_{L(f)} \frac{1}{1 + \frac{|Z_C(f)|}{R}} \\ I_{(f)} &= I_{L(f)} \frac{|Z_C(f)|}{|Z_C(f)| + R} = I_{L(f)} \frac{1}{1 + \frac{R}{|Z_C(f)|}} \end{aligned} \quad (5.20)$$

where  $I_{(f)}$  is the rms value of a sine wave current of frequency  $f$ . The above relationships can be interpreted as follows:

- the lower the capacitor's impedance for a given frequency  $f$  as related to the load resistance, the greater part of a current of this frequency  $I_{C(f)}$  will flow through the capacitor (the denominator in  $I_{C(f)}$  formula decreases, so the whole expression increases);
- thus, the smaller part  $I_{(f)}$  will flow through the receiver (the denominator in  $I_{(f)}$  formula increases, so the whole expression decreases).

In the circuit under consideration, we want to eliminate the alternating component from the  $i$  waveform. Then, the output current  $i$  will be constant and so will be the output voltage  $v$  across the load resistance (by Ohm's law). As we have noted, the direct component of the inductor current cannot flow through the capacitor, thus it entirely flows to the receiver:

$$\begin{aligned} I_{C(0)} &= 0 \\ I_{(0)} &= I_{L(0)} \end{aligned} \quad (5.21)$$

We could obtain the same result by substituting (5.19) and  $f=0$  into (5.20). How to redirect the alternating component to the capacitor? It follows from (5.20) that the condition is

$$|Z_C(f)| \ll R_L \Leftrightarrow \frac{|Z_C(f)|}{R_L} \ll 1 \quad (5.22)$$

because then

$$I_{C(f)} = I_{L(f)} \frac{1}{1 + \frac{|Z_C(f)|}{R_L}} \approx I_{L(f)} \frac{1}{1} = I_{L(f)} \quad (5.23)$$

However, capacitor impedance  $Z_C$  is dependent on frequency. As we have stated above, the inductor current AC component  $i_{L(a)}$  is of triangular shape. Based on Fourier analysis, it can be represented by a sum of sine waveforms whose frequencies are  $f_s$  and its odd multiples. Therefore, if the condition (5.22) is fulfilled for the frequency of  $f_s$ , it is also fulfilled for the entire AC component of inductor current. This is because other sine waveforms are of greater frequencies ( $3f_s$ ,  $5f_s$  etc.) and  $|Z_C|$  decreases with frequency. Thus, the entire alternating component of inductor current will flow through the capacitor. By substituting (5.19), we obtain the condition (5.22) in the form of

$$C \gg \frac{1}{2\pi f_s R_L} \quad (5.24)$$

### 5.3. Electrical quantity parameters

#### 5.3.a. Ripple factor

When DC converters are considered, ripple factor is usually defined as the ratio of the peak-to-peak ripple of the electrical quantity concerned to its direct component value. Therefore, for the inductor current, it is

$$r_i = \frac{I_{L(pp)}}{I_{L(0)}} = \frac{2\Delta i_L}{I} \quad (5.25)$$

As it can be deduced from Fig. 2.10 in Ref. B, its characteristic value is 2 as this is when the valley of the current waveform is zero. Above the value of 2, this current valley would be located below zero, but this is impossible in the considered circuit as the diode cannot conduct any reverse current. Thus, the current would be cut in its lower portion at the zero level, which would have consequences for both the power and the control circuits.

For the inductor current ripple factor, another characteristic value is between 0.3 and 0.4. It can be demonstrated that in this range, all the power components (both active and passive) are optimally loaded, i.e. their currents are well balanced and minimal and for a given converted power.

Based on the same Fig. 2.10 in Ref. B, it can be also established that the peak value of the inductor current is

$$i_{L(pk)} = I_{L(0)} + \frac{I_{L(pp)}}{2} = I + \Delta i_L \quad (5.26)$$

which in combination with (5.25) yields

$$i_{L(pk)} = I + \frac{r_i I}{2} = I \left( 1 + \frac{r_i}{2} \right) \quad (5.27)$$

A ripple factor can also be defined for the output voltage as

$$r_v = \frac{2\Delta v}{V} \quad (5.28)$$

#### 5.3.b. Mathematical description of the capacitor current waveform

As it was justified in Ref. B, Section 2.5, the capacitor current is identical with the alternating component of the inductor current. It therefore has the same triangular form and the same amplitude of  $\Delta i_L$  (see Fig. 2.26 in Ref. B). According to Eq. (2.26) in Ref. B, its positive portion corresponds to the rising portion of the voltage while its negative one, for the falling portion of the voltage.

Let us consider the time interval where the capacitor current is positive. As shown in Fig. 2.26 in Ref. B, its duration is half the  $T_s$  period. According to Fig. 2.26 in Ref. B, this positive  $i_C$  current I first linearly rising up to the value of  $\Delta i_L$  over the second half of the  $DT_s$  interval, so for a duration of  $DT_s/2$ . If we assume for simplicity that the time coordinate of  $t = 0$  corresponds to the zero of the current, then this rising process is described by:

$$i_C = \frac{\Delta i_L}{DT_s / 2} t = \frac{2\Delta i_L}{DT_s} t = m_1 t \quad (5.29)$$

To simplify the formula,

$$m_1 = \frac{2\Delta i_L}{DT_s} \quad (5.30)$$

By analogy, the linear fall of the current from  $\Delta i_L$  down to zero over the first half of the  $D'T_s$  interval, so for a duration of  $D'T_s/2$ , is described by the function:

$$i_C = \Delta i_L - \frac{\Delta i_L}{D'T_s/2}t = \Delta i_L - \frac{2\Delta i_L}{D'T_s}t = b_2 - m_2t \quad (5.31)$$

where, to simplify the formula,

$$m_2 = \frac{2\Delta i_L}{D'T_s} ; b_2 = \Delta i_L \quad (5.32)$$

### 5.3.c. Capacitor rms current

The capacitor current contains no direct component, so its average value is zero. However, this is not true for its rms value, which can be determined by applying the mathematical description obtained in Section 5.3.b.

According to the definition of the rms value,

$$I_{C(\text{rms})} = \sqrt{\frac{1}{T_s} \int_{T_s} i_C^2 dt} \quad (5.33)$$

Note that the waveform of  $i_C$  is symmetrical with respect to the time axis. Thus, due to the current being elevated to an even power, the value of the integral over the negative half-period of the current is equal to its value over the positive half-period. The latter has already been considered in Section 5.3.b where it has been divided into two intervals whose durations were  $DT_s/2$  and  $D'T_s/2$ . The same approach can be taken now, with the result being multiplied by two:

$$I_{C(\text{rms})} = \sqrt{2 \frac{1}{T_s} \left( \int_{DT_s/2} i_C^2 dt + \int_{D'T_s/2} i_C^2 dt \right)} \quad (5.34)$$

The integral over the first interval is:

$$\int_{DT_s/2} i_C^2 dt = \int_0^{DT_s/2} m_1^2 t^2 dt = \left[ \frac{1}{3} m_1^2 t^3 \right]_0^{DT_s/2} = \frac{1}{3} \left( \frac{2\Delta i_L}{DT_s} \right)^2 \left( \frac{DT_s}{2} \right)^3 = \frac{(\Delta i_L)^2 DT_s}{6} \quad (5.35)$$

while over the second one, it is:

$$\begin{aligned} \int_{D'T_s/2} i_C dt &= \int_0^{D'T_s/2} (b_2 - m_2 t)^2 dt = \int_0^{D'T_s/2} (b_2^2 - 2b_2 m_2 t + m_2^2 t^2) dt = \left[ b_2^2 t - 2b_2 m_2 \cdot \frac{1}{2} t^2 + m_2^2 \cdot \frac{1}{3} t^3 \right]_0^{D'T_s/2} = \\ &= (\Delta i_L)^2 \frac{D'T_s}{2} - \Delta i_L \frac{2\Delta i_L}{D'T_s} \left( \frac{D'T_s}{2} \right)^2 + \frac{1}{3} \left( \frac{2\Delta i_L}{D'T_s} \right)^2 \left( \frac{D'T_s}{2} \right)^3 = \\ &= \frac{(\Delta i_L)^2 D'T_s}{2} - \frac{(\Delta i_L)^2 D'T_s}{2} + \frac{(\Delta i_L)^2 D'T_s}{6} = \frac{(\Delta i_L)^2 D'T_s}{6} \end{aligned} \quad (5.36)$$

After adding up the two,

$$\begin{aligned}
 I_{C(\text{rms})} &= \sqrt{2 \frac{1}{T_s} \left[ \frac{(\Delta i_L)^2 D T_s}{6} + \frac{(\Delta i_L)^2 D' T_s}{6} \right]} = \sqrt{\frac{2(\Delta i_L)^2 T_s}{6 T_s} \cdot (D + D')} = \sqrt{\frac{(\Delta i_L)^2}{12}} \cdot 1 = \\
 &= \frac{\Delta i_L}{\sqrt{3}} = \frac{r_i I_{L(0)}}{\sqrt{3}} = I \frac{r_i}{\sqrt{3}}
 \end{aligned} \tag{5.37}$$



## 5.4. Electrical quantities at the converter's input

### 5.4.a. Input current

To determine the input power in order to analyse the circuit in respect of energy conversion, we will need to know the direct component of the input current  $i_g$ . As it can be seen in Fig. 12, and in Fig. 2.8 in Ref. B, this current is equal to the inductor current  $i_L$  over the sub-interval 1 and zero over the sub-interval 2; hence, by definition of the average value,

$$I_{g(0)} = i_{g(av)} = \frac{1}{T_s} \int_{DT_s} i_g dt = \frac{1}{T_s} \left( \int_{DT_s} i_L dt + \int_{(1-D)T_s} 0 dt \right) = \frac{1}{T_s} \int_{DT_s} i_L dt \quad (5.38)$$

Let us mathematically transform the result obtained:

$$I_{g(0)} = D \times \frac{1}{DT_s} \int_{DT_s} i_L dt \quad (5.39)$$

The expression after the multiplication sign is by definition the average value of the inductor current  $i_L$  over the time interval  $DT_s$ , i.e. the transistor's on state duration. This current's waveform is triangular (see Fig. 2.10 in Ref. B), so it consists of two sections of linear rise or fall. It is easy to show (either by simple reasoning or formally by integration) that the average value of such a waveform is simply equal to the average of the peak and valley values, and that it applies equally to the entire period and to either interval separately. Thus, the average over the  $DT_s$  sub-interval can be replaced by the average value over the entire period  $i_{L(av)}$ , or the direct component  $I_{L(0)}$ :

$$I_{g(0)} = D i_{L(av)} = D I_{L(0)} = DI \quad (5.40)$$

Using (5.21), we finally obtain:

$$I_{g(0)} = DI = D \frac{V}{R} \quad (5.41)$$

Thus, in the buck converter, the input current is less than the output current (load) by the same ratio as the output voltage is less than the input voltage [see Eq. (2.24) in Ref. B]. Taking into account (2.24) from Ref. B, the above equation may be converted to a form dependent on the input voltage:

$$I_{g(0)} = D^2 \frac{V_g}{R} \quad (5.42)$$

The resulting theoretical expression will be useful when carrying out the exercise for checking if the system is not drawing too much current, which would indicate an error or malfunction. Then, the knowledge of the theoretical input current will be needed also for the circuit from which the discussion was started, i.e. the one without passive components (Ref. B of Manual 0). In this case, the input current  $i_g$  equals the output current  $I$  over the sub-interval 1 and zero over the sub-interval 2 (cf. Fig. 1.8 in Ref. B of Manual 0). Thus, its direct component is

$$I_{g(0)} = i_{g(av)} = \frac{1}{T_s} \int_{DT_s} i_g dt = \frac{1}{T_s} \cdot \left( \int_{DT_s} i dt + \int_{(1-D)T_s} 0 dt \right) = \frac{1}{T_s} \cdot \left( \int_{DT_s} \frac{V_g}{R} dt + 0 \right) = \frac{1}{T_s} \cdot \frac{V_g}{R} DT_s = D \frac{V_g}{R} \quad (5.43)$$

A comparison of this result with (5.42) leads to the observation that for  $D < 1$ , the direct component of the input current is higher when there is no filter in the circuit. It can be easily

demonstrated that this results from the fact that the active output power in either case is also different, despite the same average value of the output voltage. Depending on the waveform—pulse wave without a filter, constant with a filter—this voltage has different rms values which is what active power depends on.

**5.4.b. Input capacitor current waveform**

Until now, we considered the input of the converter to be connected to an ideal voltage source with ideal wires. This assumption is not legitimate in reality due to a non-zero output resistance of the source and non-zero impedances of the wires. The time-varying input current  $i_g$  induces time-varying voltage drops across these resistance and impedances, which in turn causes a ripple in the input voltage  $v_g$ .

The ripple of the input voltage can be minimised with a second capacitor, connected in parallel with the input and physically located close to the terminals of the transistor and the diode. The converter’s input circuit for this case is presented in Fig. 14, where  $Z_s$  represents an equivalent impedance of the source and the connections. The input capacitor will operate similar to the output one analysed in Section 5.2.

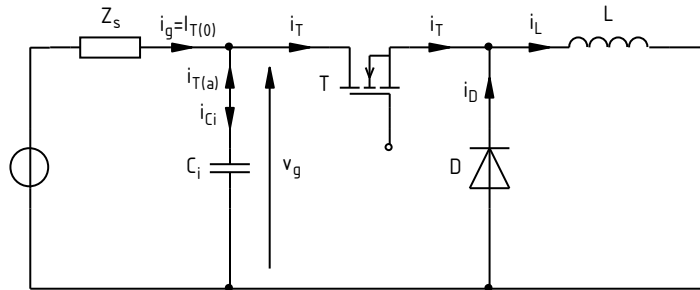


Fig. 14. Buck converter input circuit including the impedance of the source and an input capacitor

Calculations can be considerably simplified if it is assumed that the ripple of the inductor current is negligible. In such a case, the instantaneous value of this current equals its direct component, thus the load current:

$$i_L = I_{L(0)} + i_{L(a)} \approx I_{L(0)} = I \tag{5.44}$$

Under this assumption, the current of the transistor  $i_T$  is  $I$  when this transistor is on (over the  $DT_s$  interval), while it is zero when this transistor is off (over the  $D'T_s$  interval).

Currents will add in the input node as they do in the output one. By analogy, assuming that the input capacitor  $C_i$  is ideal and has an infinite capacitance, it will supply the entire alternating component  $i_{T(a)}$  of the transistor current. If current directions are marked according to the convention, i.e. the  $i_{T(a)}$  component identical to the total current  $i_T$  and the capacitor current  $i_{Ci}$  opposite to its voltage  $v_g$  (Fig. 14), this can be expressed with

$$i_{T(a)} = -i_{Ci} \tag{5.45}$$

On the other hand, as the direct component of the capacitor current must be zero (see Ref. B, Section 2.2), then the input current equals the direct component of the transistor current:

$$i_g = I_{T(0)} \tag{5.46}$$

Thus, the equation of the input node is:

$$i_T = I_{T(0)} + i_{T(a)} = i_g - i_{Ci} \tag{5.47}$$

Considering the above and Eq. (5.41), the capacitor current is:

$$i_{C_i} = i_g - i_T = I_{T(0)} - i_T = DI - i_T \quad (5.48)$$

It will therefore take values as follows:

$$i_{C_i} = \begin{cases} DI - I = (D-1)I & \text{over the } DT_s \text{ interval} \\ DI - 0 = DI & \text{over the } D'T_s \text{ interval} \end{cases} \quad (5.49)$$

Note that the former value is negative as  $D < 1$ , which corresponds to the capacitor being discharged. On the other hand, the latter is positive as  $D > 0$ . This is in line with the operating principle of the circuit. When the transistor is on (the  $DT_s$  interval), the capacitor is an additional supply source for the converter, so its current flows opposite to the  $i_{C_i}$  arrow in Fig. 14. On the other hand, when the transistor is off (the  $D'T_s$  interval), the capacitor is charged from the source.

#### 5.4.c. Input capacitor voltage ripple and rms current

The ripple of the input voltage can be related to the circuit's operating conditions and to the input capacitor's capacitance similar to the approach taken in Section 5.2 of Ref. B. The capacitor is being charged, so its voltage is rising, over the  $D'T_s$  interval. Hence, from the capacitor equation, the voltage change is:

$$\Delta v_g = \Delta u_{C_i} = \frac{\int i_{C_i} dt}{C_i} = \frac{1}{C_i} \int_{D'T_s} DI dt = \frac{DI}{C_i} \int_{D'T_s} dt = \frac{DD'T_s}{C_i} = \frac{DD'I}{f_s C_i} \quad (5.50)$$

The ripple factor of the input voltage is defined with:

$$r_{vg} = \frac{\Delta v_g}{V_g} \quad (5.51)$$

It is easy to calculate the rms value of the input capacitor current if the assumption of a negligible ripple of the inductor current is maintained. Substituting (5.49) to the definition yields:

$$\begin{aligned} I_{C_i(\text{rms})} &= \sqrt{\frac{1}{T_s} \int_{T_s} i_{C_i}^2 dt} = \sqrt{\frac{1}{T_s} \left[ \int_{DT_s} (D-1)^2 I^2 dt + \int_{D'T_s} D^2 I^2 dt \right]} = \\ &= \sqrt{\frac{1}{T_s} \left[ (D-1)^2 I^2 DT_s + D^2 I^2 (1-D)T_s \right]} = I \sqrt{(D-1)^2 D + D^2 (1-D)} \end{aligned} \quad (5.52)$$

After rearranging, the final result is obtained as:

$$I_{C_i(\text{rms})} = I \sqrt{D - D^2} = I \sqrt{DD'} \quad (5.53)$$

## 5.5. Energy-based approach to converter analysis

### 5.5.a. Average input power

By definition of the average power, the average input power is:

$$P_i = \frac{1}{T_s} \int_{T_s} v_g i_g dt \quad (5.54)$$

Assuming that the input capacitor properly fulfils its role (or, equivalently, that the supply source is ideal), the input voltage  $V_g$  can be treated as constant in time. Then,

$$P_i = \frac{1}{T_s} \int_{T_s} V_g i_g dt = V_g \cdot \frac{1}{T_s} \int_{T_s} i_g dt = V_g i_{g(av)} = V_g I_{g(0)} \quad (5.55)$$

Thus, the average input power is equal to the product of a constant input voltage and the direct component of an input current. Using (5.41), the input power can be related to the circuit's operating conditions, i.e. to the supply (the input voltage  $V_g$ ), the load (the output current  $I$ ) and the control (the duty cycle  $D$ ):

$$P_i = DV_g I \quad (5.56)$$

If we further apply Eq. (2.3) from Ref. B, we obtain:

$$P_i = D \frac{V}{D} I = VI = P_o \quad (5.57)$$

where  $P_o$  is the output power. This result proves the correctness of the calculations, as for a lossless converter—which has been the case under consideration until now—the average output power must equal the average input one.

However, this leads to the conclusion that the results obtained by now do not provide a full picture of a real circuit's operation. For a lossy circuit, the relationship (5.41) still holds and so does Eq. (5.56). On the other hand, formula (5.57) cannot be valid, because a difference appears between the input power and the output power, equal to the power loss in the converter. This discrepancy between the analysis and the reality has been introduced by Eq. (2.3) from Ref. B, which has been derived under the assumption that the switches are ideal. This means that they do not introduce any power loss, but also that no voltage drops occur across them.

### 5.5.b. Relation of voltage conversion ratio to efficiency

Producing a specific output voltage  $V$  requires a current of  $V/R$  to flow through the receiver and therefore to deliver to the output a specific power equal

$$P_o = VI = \frac{V^2}{R} \quad (5.58)$$

At an efficiency of  $\eta < 1$ , a portion of the input power is lost in the converter and therefore does not reach the receiver. If so, then the output power is less; hence, by reversing the above formula to the form

$$V = \sqrt{P_o R} \quad (5.59)$$

we come to the conclusion that the output voltage will be less than expected.

To express the above relation quantitatively, one must refer to the energy equation of the converter, i.e. to the relationship between the active input and output power. It follows directly from the definition of efficiency:

$$P_i = \frac{P_o}{\eta} \quad (5.60)$$

Assuming a constant input voltage, the active input power  $P_i$  is given by equation (5.55), while the output power is expressed with equation (5.58). The above equation can therefore be expanded to

$$V_g I_{g(0)} = P_i = \frac{P_o}{\eta} = \frac{VI}{\eta} \quad (5.61)$$

As we stated in Section 5.4.a, the input current is equal to the inductor current for the time the transistor is on, which is what we derived (5.40) from. That relationship is also valid for a lossy converter, as it was derived from Kirchhoff's current law applied to the node in which the semiconductor switch connects to the inductor; it must be always maintained, regardless of energy loss in the system. In turn, from Kirchhoff's current law for the output node and from the assumption of ideal filtration, we obtained (5.21). Both currents (the input and the output ones) can therefore be expressed through the direct component of the inductor current:

$$V_g D I_{L(0)} = \frac{VI_{L(0)}}{\eta} \quad (5.62)$$

Hence, after transformation, we obtain the voltage conversion ratio (denoted  $M$  in Ref. B) as:

$$K_U = \frac{V}{V_g} = \eta D \quad (5.63)$$

By comparing the above result to the voltage conversion ratio for the ideal (lossless) converter (see Ref. B)

$$K_{U(id)} = D \quad (5.64)$$

we find that the voltage conversion ratio for the real (lossy) buck converter is lower by a ratio equal to this converter's efficiency:

$$K_U = \eta K_{U(id)} \quad (5.65)$$

In other words, if some specific voltage  $V_g$  is applied at the converter's input and a the transistor is controlled with a signal of a specific duty cycle  $D$ , then the output voltage obtained in a real buck converter will be less than that in an ideal converter by a ratio equal to the efficiency of the former.

### 5.5.c. The impact of power loss on the current input

Finally, let us return to the discussion started in Section 5.4.a. The result obtained there [equation (5.42)] can also be reached by means of energetic analysis, which is even simpler because by transforming (5.61), we directly get

$$I_{g(0)} = \frac{P_o}{\eta V_g} = \frac{V}{V_g} \frac{I}{\eta} = I \frac{K_U}{\eta} \quad (5.66)$$

The obtained relationship is in fact a generalisation of equation (5.40), which can be seen when (5.63) is substituted into the latter. That equation is valid only for a specific topology: the buck converter. In contrast, the energy equation (5.61) and the relationship (5.66) are universal: true not

only for the real (lossy) buck converter but also in general for any DC converter. This is because the relationships used to derive them were not linked to any specific circuit topology, nor were they founded on the assumption of unit efficiency.

Formula (5.66) allows the designer to predict the input current necessary to convert the voltage at a given ratio  $K_U$ , at a given load  $I$  and an assumed efficiency  $\eta$ . It tells that the direct component of the input current is:

- 1° proportional to the output current by a ratio inverse to the ratio of voltages ( $I_{g(0)} / I \propto V / V_g$ ),
- 2° inversely proportional to the converter efficiency (which is a number less than 1 so dividing by it means increasing the result).

Thus, the converter will draw a greater input current (meaning the direct component) for:

- 1° a higher output to input voltage ratio, which means that when a converter steps down the voltage, then the input current is less than the output current, and vice versa,
- 2° a less efficient inverter, which follows directly from the energy equation (5.61) because for a given input voltage  $V_g$ , if efficiency  $\eta$  is lower, then delivering a given output power  $P_o$  requires a greater input current to flow in order for the left-hand and the right-hand sides of the equation to match.

## 6. Pulse wave generator

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### 6.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
D	[19]	Monostable operation; Astable operation	6.1, 6.2		6.2

## 6.2. Modified configuration

### 6.2.a. Basic astable configuration using a potentiometer

In [19], formulae have been derived for the charge  $t_{\text{ch}}$  and discharge  $t_{\text{dch}}$  times in the case of astable operation:

$$t_{\text{dch}} = 0,693\tau_{\text{dch}} = 0,693R_2C \quad (6.1)$$

$$t_{\text{ch}} = 0,693\tau_{\text{ch}} = 0,693(R_1 + R_2)C \quad (6.2)$$

where  $\tau_{\text{ch}}$  and  $\tau_{\text{dch}}$  are the exponential charge and discharge time constants. These formulae, together with general relationships for pulse (or switching in the future) frequency  $f_p$  and duty cycle  $D$ ,

$$f_p = \frac{1}{T_p} = \frac{1}{t_{\text{ch}} + t_{\text{dch}}} \quad (6.3)$$

$$D = \frac{t_{\text{ch}}}{T_p} = \frac{t_{\text{ch}}}{t_{\text{ch}} + t_{\text{dch}}} \quad (6.4)$$

enabled deriving the final relationships that can be used in design:

$$f_p = \frac{1}{0,693(R_1 + 2R_2)C} \quad (6.5)$$

$$D = \frac{R_1 + R_2}{R_1 + 2R_2} \quad (6.6)$$

It is self-evident to change the  $D$  ratio using a potentiometer, such as  $R_2$  in Fig. 17. In such a case,  $R_1$  and  $R_2$  represent the currently set resistances of the first and second sections of the potentiometer, and their sum is always constant and equals the potentiometer total resistance:

$$R_1 + R_2 = R_p = \text{const} \quad (6.7)$$

which follows from the mechanical design of this component. Let us denote the current potentiometer's division ratio with  $k$ ,

$$k = \frac{R_1}{R_1 + R_2} = \frac{R_1}{R_p} \quad (6.8)$$

Then,

$$D = \frac{2k - 1}{3k - 2} \quad (6.9)$$

$$f_p = \frac{1}{0,693(3k - 2)(R_1 + R_2)C} = \frac{1}{0,693(3k - 2)R_p C} \quad (6.10)$$



### 6.2.b. Improved astable configuration

An analysis of the relationships (6.9) and (6.10) leads to the conclusion that the basic astable circuit has three considerable drawbacks:

- (1) the frequency is dependent on the current potentiometer wiper position,
- (2) the duty cycle is a non-linear function of the wiper position,
- (3) it is only possible to obtain  $D$  values from the (0,5; 1) range.

It can be easily stated that the cause for the above problems is that the capacitor is discharged through only one of the resistors while it is charged through both. These drawbacks can be eliminated by inserting a diode in parallel to the bottom section of the potentiometer (see Fig. 15). Then, charging proceeds only through the  $R_1$  resistor. Neglecting the voltage drop across the diode, we obtain

$$t_{\text{ch}} = 0,693\tau_{\text{ch}} = 0,693R_1C \quad (6.11)$$

Discharge still proceeds in the same way, so equation (6.1) stays valid. Thus

$$D = k \quad (6.12)$$

$$f_p = \frac{1}{0,693(R_1 + R_2)C} = \frac{1}{0,693R_pC} = \text{const} \quad (6.13)$$

Square wave frequency therefore becomes invariant as it depends on the sum of  $R_1$  and  $R_2$  resistances that is constant and equals the potentiometer resistance  $R_p$ .

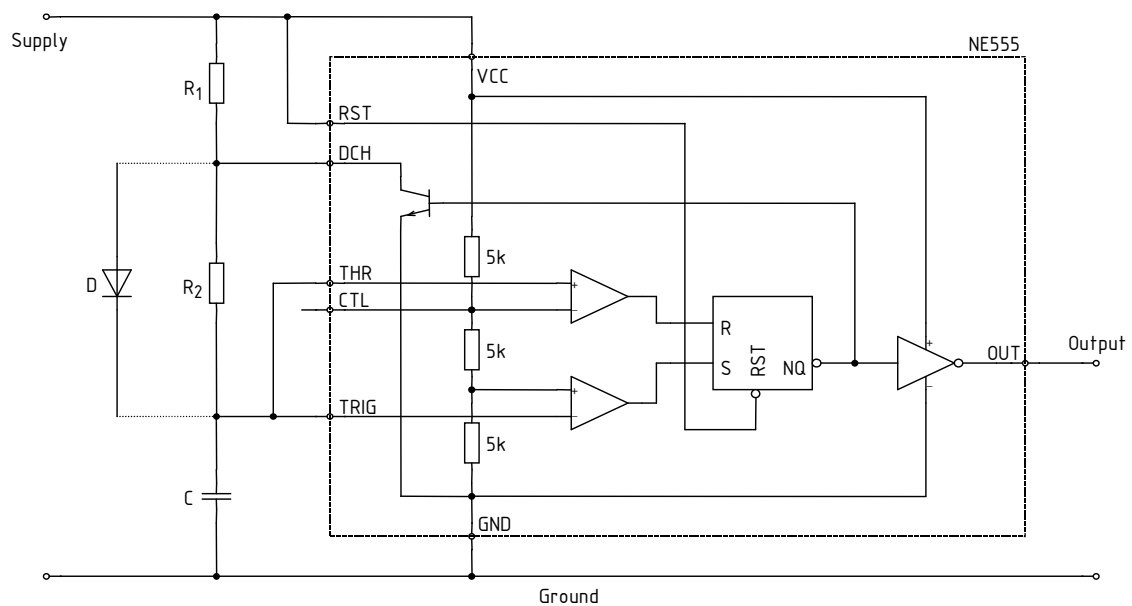


Fig. 15. Schematic of the 555 timer integrated circuit showing the external component connections with the optional diode

Characteristics of a real circuit will differ from the above due to several factors such as non-zero and  $k$ -dependent voltage drops across a conducting diode and a conducting discharge transistor, or changes of the  $U_{CC}$  voltage following changes of the duty cycle.

### 6.2.c. Application circuit

The circuit analysed above basically corresponds to the one of Fig. 17 with the following provisions:

- the resistor  $R_1$  corresponds to the total resistance in the path of the charge current, thus of the resistor  $R_1$ , the upper section of the potentiometer  $R_2$  and the resistor  $R_3$ ;
- the resistor  $R_2$  corresponds to the total resistance in the path of the discharge current, thus of the lower section of the potentiometer  $R_2$  and the resistor  $R_3$ ;
- the capacitor  $C$  is the capacitor  $C_2$ .

The task of the  $R_1$  and  $R_3$  resistors is to limit the duty cycle  $D$  so that the full range of  $[0; 1]$  is not achieved. Operation in regions close to 0 or 1 would cause a hard to predict circuit behaviour. Due to the non-zero switching times of the semiconductor switch, there is some low value of  $D$  for which the transistor stops to switch even though the driving pulse duty cycle is still greater than zero. By analogy, starting from some high value of  $D$ , the transistor will be constantly on even though the driving signal is not yet constant. Operation in some ranges (that cannot be precisely determined now) neighbouring 0 and 1 makes it therefore impossible to vary the lamp light intensity. Additionally, values of  $D$  that are close to the above mentioned boundaries would normally cause an unstable circuit operation: changing light intensity, toggling between on and off, etc.

After applying the symbols of Fig. 17 to the formulae (6.1) and (6.11), we obtain:

$$t_{\text{dch}} = 0,693(R_{2\text{d}} + R_3)C_2 \quad (6.14)$$

$$t_{\text{ch}} = 0,693(R_1 + R_{2\text{g}} + R_3)C_2 \quad (6.15)$$

where the upper section's resistance of the  $R_2$  potentiometer has been denoted as  $R_{2\text{g}}$  and the lower section's one as  $R_{2\text{d}}$ .

Substituting the above to the relationship (6.3), we get the formula for the rectangular waveform frequency in the designed circuit:

$$f_p = \frac{1}{t_{\text{ch}} + t_{\text{dch}}} = \frac{1}{0,693(R_1 + R_{2\text{g}} + R_3)C_2 + 0,693(R_{2\text{d}} + R_3)C_2} \quad (6.16)$$

Considering that the sum of both potentiometer sections' resistances is constant and equals its total resistance  $R_4$ , the above can be simplified to the form of

$$f_p = \frac{1}{0,693(R_1 + R_2 + 2R_3)C_2} \quad (6.17)$$

Next, from (6.4) we obtain

$$D = \frac{t_{\text{ch}}}{t_{\text{ch}} + t_{\text{dch}}} = \frac{0,693(R_1 + R_{2\text{g}} + R_3)C_2}{0,693(R_1 + R_{2\text{g}} + R_3)C_2 + 0,693(R_{2\text{d}} + R_3)C_2} = \frac{R_1 + R_{2\text{g}} + R_3}{R_1 + R_2 + 2R_3} \quad (6.18)$$

The minimum and the maximum duty cycle will be obtained by setting the potentiometer's wiper in either of its extreme positions. For the wiper in its extreme top (according to Fig. 17) position, we have  $R_{2\text{g}} = 0$ , so

$$D_{\text{min}} = \frac{R_1 + R_3}{R_1 + R_2 + 2R_3} \quad (6.19)$$

Whereas for the extreme bottom position,  $R_{2g} = R_2$ , so

$$D_{\max} = \frac{R_1 + R_2 + R_3}{R_1 + R_2 + 2R_3} \quad (6.20)$$

### 6.2.d. Current consumption

In order to design the generator, we will additionally estimate the required supply current. For the logic part of the integrated circuit, current consumption is given in its data sheet. Still, the auxiliary circuit  $R_1$ – $R_2$ – $C$  together with the discharge transistor must be considered. The current drawn by this circuit is synonymous to the  $R_1$  resistor current  $i_{R_1}$ .

During the capacitor charge phase, current decreases exponentially from a certain initial value down to zero. The initial, maximum current value equals initial voltage across the  $R_1$  resistor divided by its resistance; while it follows from the previous analysis that the voltage across the capacitor is  $\frac{1}{3}U_{CC}$  at that moment. Thus,

$$i_{R_1(\text{ch})}(t=0) = \frac{U_{CC} - \frac{1}{3}U_{CC}}{R_1} = \frac{2}{3} \frac{U_{CC}}{R_1} \quad (6.21)$$

During the discharge phase, current is drawn from the supply only because of the DCH pin being shorted to ground by the transistor which is on. Thus, its value is (after neglecting the voltage drop across the transistor)

$$I_{R_1(\text{dch})} = \frac{U_{CC}}{R_1} \quad (6.22)$$

A maximum average value (over the  $T_p$  period) of the current drawn from the supply will therefore occur when the discharge phase duration is maximum which means  $D = D_{\min}$ ,  $R_1 = R_{1(\min)}$ . To avoid precise calculation of the average value of the current during the charge phase, we will overestimate it by assuming that it is constant. Then,

$$I_{R_1(\text{av})\max} \approx (1 - D_{\min}) \cdot \frac{U_{CC}}{R_{1(\min)}} + D_{\min} \cdot \frac{2}{3} \frac{U_{CC}}{R_{1(\min)}} = \left(1 - \frac{D_{\min}}{3}\right) \cdot \frac{U_{CC}}{R_{1(\min)}} \quad (6.23)$$

where  $R_{1(\min)}$  is the minimum value of the resistance  $R_1$  that can occur in a given application circuit. In the practical circuit of Fig. 17, this occurs when the wiper of the potentiometer  $R_2$  is in its extreme top position and equals  $R_1$  because  $R_{2g} = 0$  then.

Under the assumption that  $D_{\min}/3 \ll 1$ , the above formula can be simplified to

$$I_{R_1(\text{av})\max} \approx \frac{U_{CC}}{R_{1(\min)}} \quad (6.24)$$

so using symbols of Fig. 17 it becomes

$$I_{R_1(\text{av})\max} \approx \frac{U_{CC}}{R_1} \quad (6.25)$$



## 7. Thermal Phenomena in Semiconductor Devices

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### 7.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
E	Moh	29-1, 29-2, 29-2-1, 29-2-2, 29-3, 29-4, 29-4-1, 29-4-2	7.1, 7.2, 8.2.c, 8.3.a,c, 8.4	[14]* 7.1.1 (The power dissipation limit, Continuous power dissipation, Pulse power operation, Short pulse duration, Long pulse duration, Periodic rectangular pulse), 7.1.2 (Heat flow path, Thermal resistance calculations, Continuous operation, Intermittent operation) [16] 5	
F	Ben	2.1.4	7.3.a–d		

\* Ref. [14] has already been published for Manual 5U.



## 8. VDMOS Safe Operation

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### 8.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
G*	Ben	10.4	7.3.e–f, 8.1, 8.2, 8.3.b, 8.4.b, 8.5.a–c	[14]** 1.2.1 (The Safe Operating Area), 1.2.7 (Introduction, Failure mechanism of a non-rugged Power MOS, Definition of ruggedness), 1.2.9 (Quick reference data, Limiting values, Static characteristics, Safe Operating Area, Calculating currents), [15] 1–4 [16] 1–3	
H***	Ben	6.2.4, 6.4, Fig. 6.6	7.3.e–f, 8.1.a, 8.2.d	[14] 2.1.2 (Safe Operating Area), Fig. 10	
I	Moh	27-4	8.5.d	[17] 4	

\* Ref. G is found in the document already published as Refs. ABC for Manual 3P; the Fig. 3.19 referenced there is found in Ref. H for Manual 0.

\*\* Ref. [14] has already been published for Manual 5U.

\*\*\* Ref. H is found in the document already published as Refs. AB for Manual 5P.





## 9. Electronic design

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### 9.1. Practical circuit

#### 9.1.a. Transistor drive

To obtain a complete converter circuit, the power circuit analysed in Chapter 5 must be coupled with the control circuit presented in Chapter 6. It should be however noted that that generator provides a voltage waveform referenced to the ground, while the MOSFET in Fig. 11d is driven with respect to another potential: the cathode of the diode D. This is because it is the gate-source voltage  $u_{GS}$  which is the controlling quantity for this transistor, but its source is not connected to the ground of the considered circuit. An even higher complexity results from the fact that this transistor's source potential is time-varying due to the periodical switching of the diode D. Fig. 2.8 in Ref. B shows that the magnitude of these variations is large: between approximately zero when the diode is on, and the input voltage  $V_g$  when the transistor is on.

The most universal solution to the above problem is to introduce a level shifter able to operate with a variable reference potential. Such a shifter can be assembled from discrete components, or a dedicated integrated gate driver can be used. However, the former approach would considerably increase the component count as well as make it necessary to commission and test an additional functional block, while the latter would significantly raise the circuit's cost.

For these reasons, the simplest solution has been chosen for the present exercise, based on Kirchhoff's current law in its cut-set formulation (stating that the sum of currents of all the branches belonging to any cut-set of a circuit is zero). A cut-set of the circuit presented in Fig. 11d is, for example, formed by the branch containing the MOSFET and the corresponding ground wire below as well as by the branch containing the inductor and its corresponding ground wire below. This means that the currents flowing in the return wires that make up the bottom side of the rectangle formed by the circuit's schematic are identical to the currents flowing through the corresponding components that make up the upper side of this rectangle.

Consequently, exchanging these components and their corresponding return wires will not modify the circuit's operation in any way (as long as an ideal circuit is considered). A schematic of the buck converter after such an exchange is done is presented in Fig. 16.

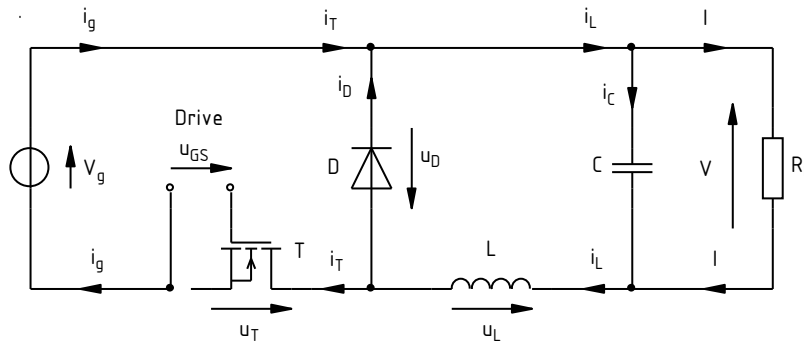


Fig. 16. Modified buck converter circuit schematic with transistor drive referenced to the ground of the source

The modified circuit has a significant limitation: it cannot be used with loads that need to be supplied with respect to the negative terminal of the source  $V_g$ . This is because the modification introduced resulted in a separation of the input and output grounds (understood here as the respective negative terminals). The requirement of a common ground concerns, e.g., any appliances composed of several modules where some part of them is supplied with the voltage  $V_g$  while some, with the voltage  $V$ , and different modules have to communicate with each other. On the other hand, if the load is autonomous and does not use wired communication with its environment, then using the circuit variant with the ground-referenced transistor drive is both possible and advantageous thanks to its simplicity. Such applications include light sources and wireless sensors among others.

### 9.1.b. Detailed practical schematic diagram and functional blocks

The ultimate electrical schematic of the complete circuit, including the source and the load, is presented in Fig. 17. The standard subscripts “i” and “o” indicate input and output quantities, respectively, instead of “g” and blank subscript used throughout Ref. B and Chapter 5 of this manual. The portion between the dashed lines will be the object of design and assembly in this exercise.

The complete converter is composed of the following functional blocks.

1. **Input filter:** the capacitor  $C_1$ .

Its role is to provide a constant supply voltage as well as to eliminate the influence of resistances and inductances of the wires connecting the supply source to the converter's input. An electrolytic capacitor will be used due to the large capacitance required for this purpose.

2. **Control block:** pulse wave generator based on the integrated circuit  $U_1$  and the potentiometer  $R_2$ .

The NE555 generates a pulse wave of some frequency and duty cycle. Both these parameters result from the capacitance of the capacitor  $C_2$ , the constant resistances of  $R_1$  and  $R_3$  as well as from a present setting of the potentiometer  $R_2$ . The diode  $D_1$  has been added to make the waveform frequency independent of the potentiometer's setting. Due to the high stability of capacitance required (e.g. with respect to temperature), a monolithic capacitor will be applied. The operation of this generator for the configuration used has been analysed in detail in Sub-chapter 6.2.

The capacitors  $C_3$  and  $C_4$  are used to de-couple the control circuit, i.e. to minimise any external influence on the operation of the NE555. In the circuit under consideration, their principal task is to prevent high-frequency disturbances generated in the power block as a result of the transistor's switching from interfering with the operation of the control block. This goal is achieved by filtering the supply voltage of the integrated circuit (VCC pin,

capacitor  $C_3$ ) as well as of its internal voltage reference (CTL pin, capacitor  $C_4$ ). Due to low capacitances and their wide tolerances allowed but still a low parasitic inductance required, standard ceramic capacitors will be used.

At the same time, the NE555 fulfils the role of a gate driver for the MOSFET, making it possible to supply a required change in a sufficiently short time. It should be recalled that just generating a voltage at the output of a generator is not enough to turn on a MOSFET; in addition, a sufficient current flow must be enabled to charge the transistor's input capacitance to reach the required voltage level between its gate and source terminals, or to discharge this capacitance to turn off the transistor. Thanks to its bipolar structure, the variant of the NE555 used enables a sufficiently high current to be sourced or sunk at its output (OUT pin) for this purpose.

The control circuit is completed with the resistor  $R_4$  which sets the value of the gate current and thus, the switching speed of the transistor.

3. **Power block**, where the control signal (here,  $u_g$ ) is translated into specific actions resulting in appropriate changes in the load loop (here, the switching of the current of the inductor  $L_1$ ).

The actuator that performs the above function is the SPDT switch composed of the MOSFET  $Q_1$  (in the low-side switch configuration) and the diode  $D_2$ . The electrolytic capacitor  $C_5$  filters the output voltage, ensuring that it stays constant over every switching period of the converter. The choke (inductor)  $L_1$  ensures the continuity of the current flow and at the same time supports the capacitor  $C_1$  in its output filter role (which filter may therefore be considered an LC one). Due to the high inductance required for this purpose, a component with a magnetic core must be used.

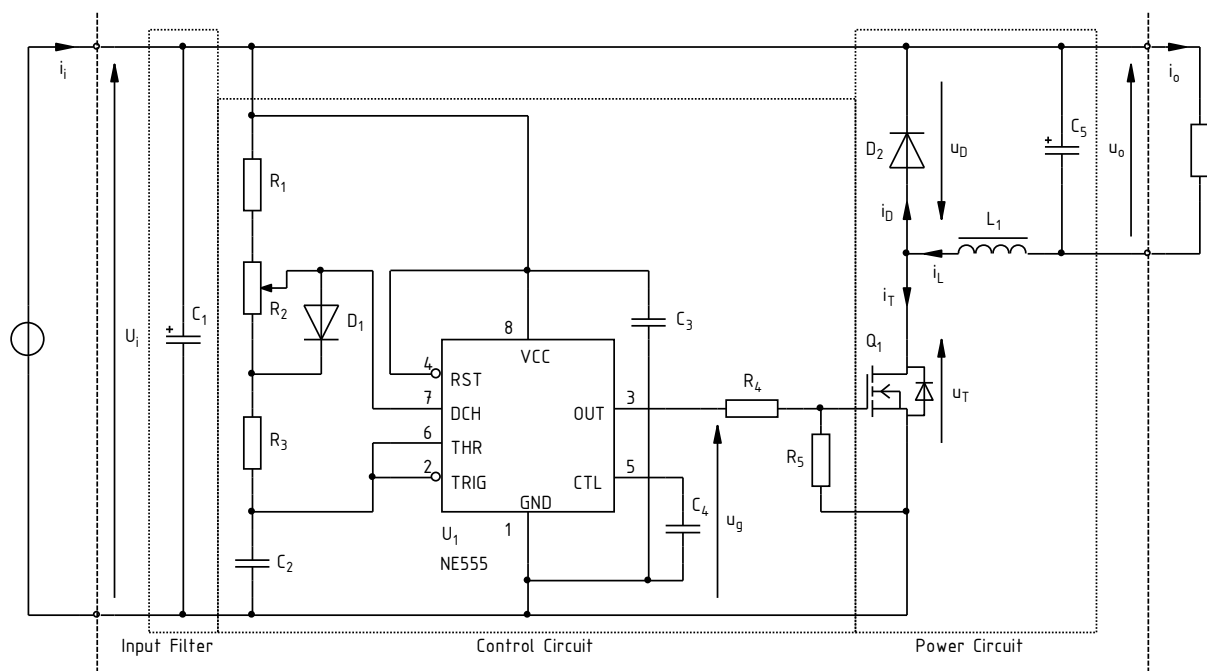


Fig. 17. Complete electrical schematic of the buck converter including its control circuit

### 9.1.c. Gate-source resistor

Due to its being connected to the gate, the resistor  $R_5$  is part of the control block. This component minimises the effect of disturbances on the MOSFET's operation. Such disturbances come in from the power loop through this transistor's parasitic capacitance  $C_{GD}$  and may lead to its undesirable turn-on or turn-off as a result of an excessive voltage rise or fall between its gate and

source. When a resistor is inserted with a sufficiently low impedance (lower than that of the parasitic capacitance  $C_{GS}$ ), any additional charge related to the propagation of disturbances will be brought to the ground through this resistor instead of being accumulated in  $C_{GS}$  and thus increasing the  $u_{GS}$  voltage.

A second task of the resistor  $R_5$  is to prevent the transistor from turning on undesirably should the drain circuit be supplied when no gate drive is present (as a result of e.g. a gate driver failure or a circuit continuity interruption). In such a case, the high  $U_{DS}$  voltage would become divided by the divider formed by the parasitic capacitances  $C_{GD}$  and  $C_{GS}$ . Consequently, a non-zero  $u_{GS}$  voltage would emerge, which could turn on the transistor in an uncontrolled way, which in turn could lead to its being destroyed as a result of excessive power dissipation.

It should be noted that the presence of the resistor  $R_5$  decreases the magnitude of the gate-source voltage  $u_{GS}$  as compared to the generator voltage  $u_g$ . This is because the  $u_g$  voltage is divided by the resistive divider formed by  $R_4$  and  $R_5$ .

## 10. Printed Circuit Board Design

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### 10.1. General assumptions

#### 10.1.a. Electrical connection schematic of the board

Figure 17 contains components that do not belong to the converter (the source, the load). On the other hand, some additional components are not represented there that will have to be included in the real circuit for practical reasons.

The ultimate schematic with the complete set of components that will be found on the circuit's board is presented in Fig. 19 (p. 63). In comparison to Fig. 17, the following changes have been introduced there:

- the supply source has been omitted as it does not belong to the converter; instead, a connector (terminal block)  $J_1$  has been provided to connect the input voltage brought from this power supply  $U_i$ ;
- the load has been omitted as it does not belong to the converter and will be external to the board; instead, a connector (terminal block)  $J_2$  has been provided to connect a load;
- the terminals of the potentiometer  $R_2$  have been distinguished to emphasize that this component can be located outside the board, connected with three separate wires;
- a heat sink  $HS_1$  has been added that can be necessary for the transistor  $Q_1$ ;
- measurement points have been provided to connect voltage probes:  $P_1$  for their ground clips and  $P_2$  for the continuous measurement of the  $u_{GS}$  voltage which will serve as a synchronising signal for the oscilloscope; at these locations, a bare wire of an appropriate length will be soldered to a track on the board;
- measurement wires  $W_1$  to  $W_3$  have been provided to clamp a current probe to measure diode, transistor and inductor currents; at these locations, an insulated wire of an appropriate length will be soldered between two tracks on the board.

The ultimate component list is contained in Table 2 (p. 64). The following data are provided there:

- component symbol according to Figs. 17 and 19,
- component kind,
- component type, value or other parameters,
- case type or its parameters,
- reference to case picture,

- sketch of case footprint with a basic arrangement of component leads on a universal board (where white squares represent soldering holes and pads),
- lead spacing (a minimum and a maximum one are given where leads can be bent or cut); the numbers between parentheses indicate absolute minimum values.

### 10.1.b. Universal printed circuit board used

In the present exercise, a UM-8 universal prototyping printed circuit board may be used (see Sub-chapter 2.1). Its picture has already been shown in Fig. 2 (p. 12). A simplified layout of traces soldering pads is shown in Fig. 18. The pitch of this board is 2.5 mm and its dimensions are 70 mm × 50 mm.

The UM-8 board is has two possible variants. One of them has 10 full columns (i.e. where each vertical trace contains three soldering holes) in either half; whereas the second one has 11 such columns. Fig. 18 corresponds to the lower column number variant. Both versions are implemented in the worksheet used in this exercise.

The information about the board variant used in a given year is published on the course web page together with the worksheet description. In the case this information is missing at the start of the design process, it should be performed for the board with 10 full columns. This will enable realising the design without any problem independent of which variant is received later. In the case of the 11-column variant, one should only remember not to use the two opposite columns closest to the board centre.

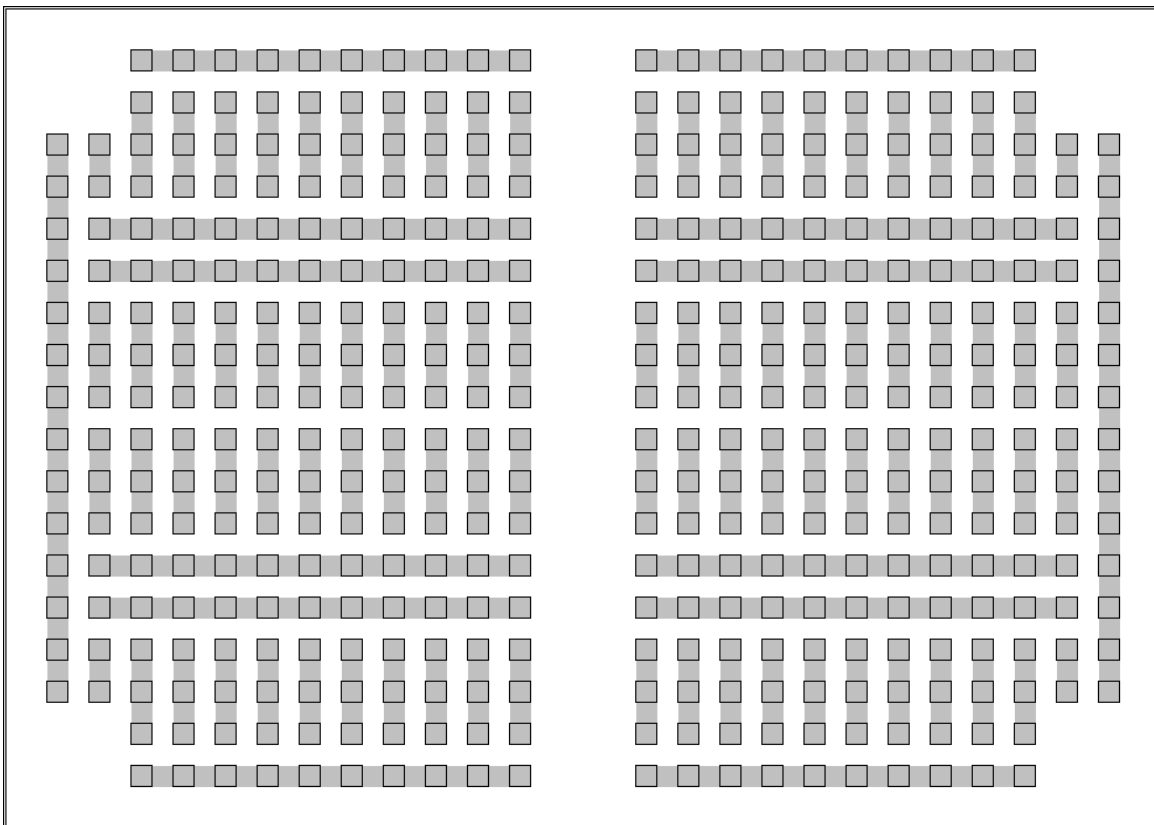


Fig. 18. A simplified image of conducting trace and solder pads layout for the UM-8 board with 10 full columns (squares with a black frame represent solder pads, while grey areas represent conducting traces)

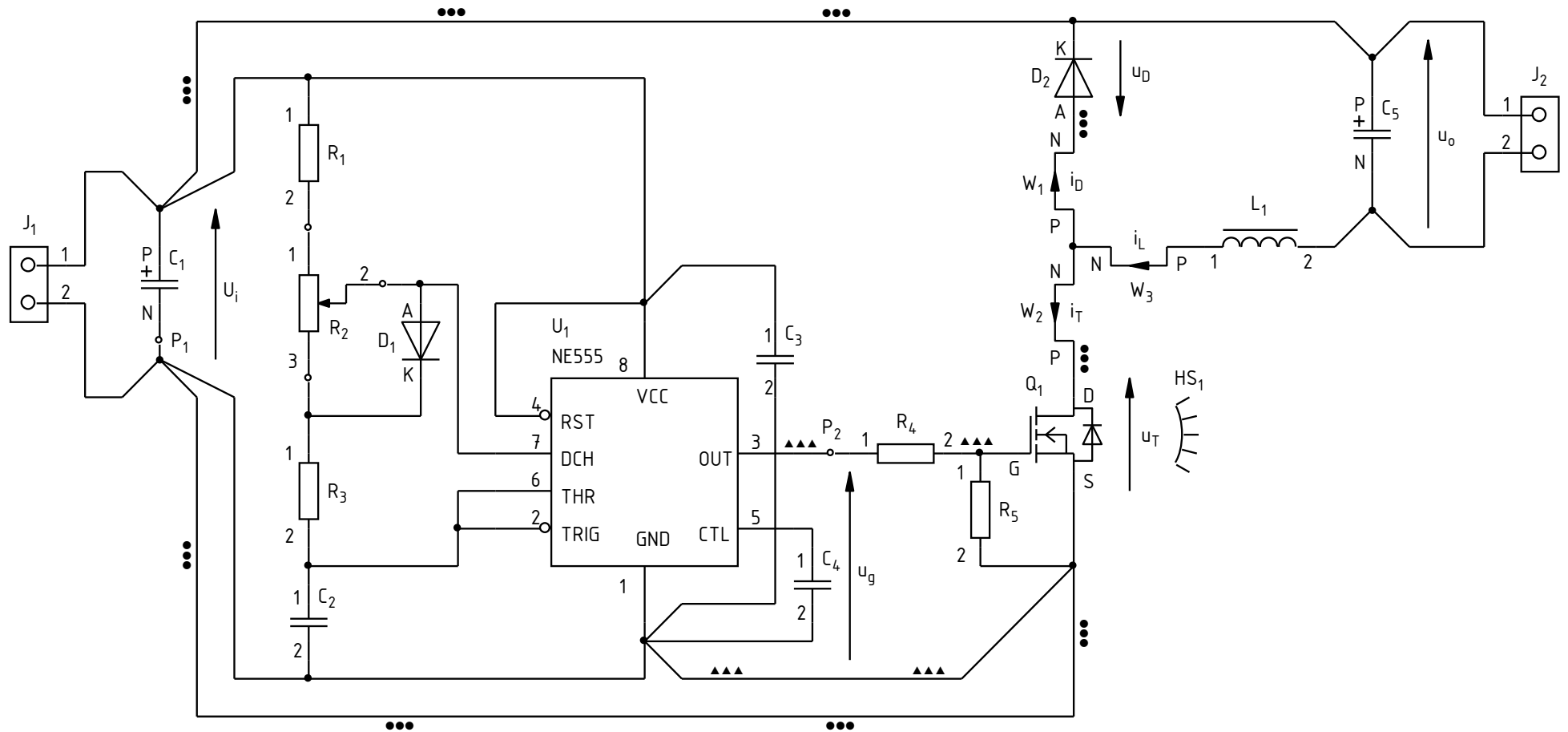


Fig. 19. Complete electrical schematic of the circuit's board

Table 2. Required component list for assembling the circuit

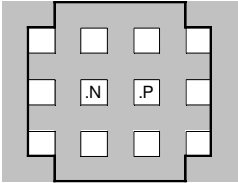

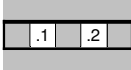
Designator	Component	Value Type Parameters	Case	Fig. 1 <sup>1</sup>	Sketch of case footprint and lead arrangement on the universal board	Lead spacing
C <sub>1</sub>	Capacitor, aluminium electrolytic	⊠ μF, ⊠ V, ⊠ mA, 105 °C	Vertical cylindrical; depending on electrical parameters: min. ∅ 5, R 2,0 max. (see drawing) ∅ 8, R 3,5	d-1		1r...10r
C <sub>2</sub>	Capacitor, monolithic ceramic	⊠ μF, 50 V		d-3		(1r) 2r...10r
C <sub>3</sub>	Capacitor, disc ceramic	100 nF, 50 V		d-4		1r...8r
C <sub>4</sub>	Capacitor, disc ceramic	10 nF, 50 V	As for C <sub>3</sub>			
C <sub>5</sub>	Capacitor, aluminium electrolytic	⊠ μF, ⊠ V, ⊠ mA, 105 °C	As for C <sub>1</sub>			



Table 2. Required component list for assembling the circuit

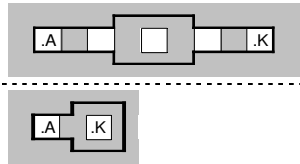
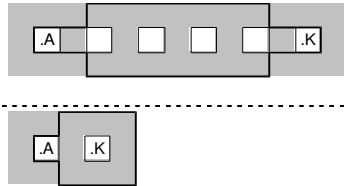
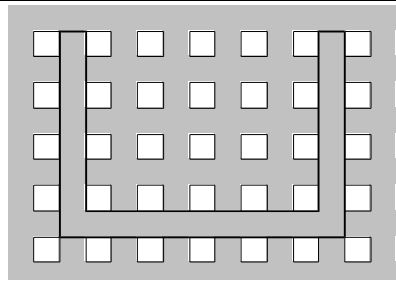
Designator	Component	Value Type Parameters	Case	Fig. 1 <sup>1</sup>	Sketch of case footprint and lead arrangement on the universal board	Lead spacing
D <sub>1</sub>	Small-signal diode, fast switching	1N4148 200 mA, 100 V, 8 ns	DO-35 Horizontal mount	e-1		4r...18r
			Vertical mount			1r...4r
D <sub>2</sub>	Power diode, Schottky	$\diamond$ $\diamond$ A, $\diamond$ V, < 100 ns	min. DO-41, max. (rys.) DO-15 Horizontal mount	e-2		(4r) 5r...18r
			Vertical mount			1r...4r
HS <sub>1</sub>	Heat-sink, moulded		U-shaped, for TO-220 case, max. 13,3 mm × 9,6 mm			—

Table 2. Required component list for assembling the circuit

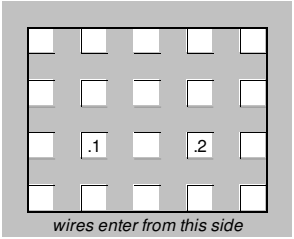
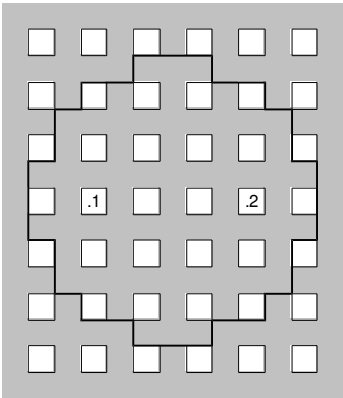

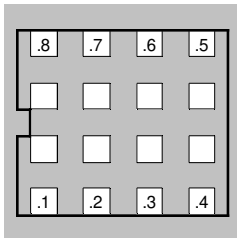

Designator	Component	Value Type Parameters	Case	Fig. 1 <sup>1</sup>	Sketch of case footprint and lead arrangement on the universal board	Lead spacing
J <sub>1</sub> J <sub>2</sub>	Screw terminal block	2-pin	Horizontal wire orientation; R 5,0	k		2r
L <sub>1</sub>	Power choke	◇ μH, ◇ A	Vertical cylindrical; depending on electrical parameters: min. ∅ 7,5, R 3,0 max. (see drawing) ∅ 12,5, R 7,0			(1r) 2r...10r
P <sub>1</sub> P <sub>2</sub>	Measurement point			—		—

Table 2. Required component list for assembling the circuit

Designator	Component	Value Type Parameters	Case	Fig. 1 <sup>1</sup>	Sketch of case footprint and lead arrangement on the universal board	Lead spacing
Q <sub>1</sub>	Power transistor, MOSFET	$\diamond$ $\diamond A, \diamond V$	TO-220 <sup>2</sup>	g-3	<p>back side, base</p>	$2 \times 1r^3$
R <sub>1</sub>	Resistor, carbon	$\diamond \Omega, (0,125...0,6) W$	Horizontal mount	a-2 a-3 a-4		$5r...20r$
			Vertical mount			$1r...4r$
R <sub>2</sub>	Potentiometer, axial	$\diamond \Omega, \text{linear}$	Mounted at the board's edge <sup>2</sup>	c-1		$2 \times 2r$
			Located outside the board		<p>Connected to the board with three separate wires</p>	Any
R <sub>3</sub>	Resistor, carbon	$\diamond \Omega, (0,125...0,6) W$	As for R <sub>1</sub>			

Table 2. Required component list for assembling the circuit

Designator	Component	Value Type Parameters	Case	Fig. 1 <sup>1</sup>	Sketch of case footprint and lead arrangement on the universal board	Lead spacing
R <sub>4</sub>	Resistor, carbon	⊠ Ω, (0,5...1) W		a-3	As for R <sub>1</sub>	
R <sub>5</sub>	Resistor, carbon	(10...100) kΩ, (0,125...0,6) W	As for R <sub>1</sub>			
U <sub>1</sub>	Integrated circuit, timer	NE555	DIP-8	h	Socket-mounted	
	Integrated circuit socket	Standard	DIP-8	i-2		X-axis: 3 × 1r Y-axis: 3r
W <sub>1</sub> W <sub>2</sub> W <sub>3</sub>	Measurement wire					(1r) $\frac{7r...29r}{4}$

- ⊠ – Parameter to be selected
- r – UM-8 universal PCB pitch = 2,5 mm
- ∅ – Diameter in millimetres
- R – Lead pitch in millimetres

<sup>1</sup> The photograph depicts a case of an identical shape, but its dimensions can be different.

<sup>2</sup> The outer footprint corresponds to the case body located at 4 mm minimum above the board. It can be assumed that the area occupied of the board's surface corresponds to the inner footprint.

<sup>3</sup> Each lead can be bent forward or backward by 2r maximum; the G lead can be bent to the left by 2r maximum; the S lead can be bent to the right by 2r maximum.

<sup>4</sup> With a distance of 16 mm ≈ 7r, the current probe will fit between the mounting points of the wire ends. However, this wire can form a loop wider than the mounting points spacing which can be arbitrarily small then.

## 10.2. The real character of electrical connections

### 10.2.a. Effect of physical connections on circuit operation

Apart from the changes enumerated above, the new schematic is different from the one of Fig. 17 in one important aspect. It takes into account (at its most important points) physical, and not abstract, electrical connections.

In an abstract schematic, we assume that each line symbolising an electrical connection is equipotential (an identical electrical potential appears along its entire length), so it represents a short-circuit. However, this is not true in real circuits, especially where high and fast varying currents are flowing. Each elementary section  $\delta l$  of a conductor has some non-zero elementary resistance  $\delta R$  and some elementary inductance  $\delta L$ . According to Ohm's law, a current flowing through such a conductor causes voltage drops to appear across these elementary resistances:

$$\delta u_R = \delta R \cdot i \quad (10.1)$$

while rapid variations of this current cause voltage drops to appear across the elementary inductances, according to the coil formula:

$$\delta u_L = \delta L \cdot \frac{di}{dt} \quad (10.2)$$

In power electronic circuits we deal with both high currents  $i$  and high rates of change  $di/dt$ , so important voltage drops may arise in conductors.

Drops across resistances are usually not significant, so they do not have visible negative effects on the operation of circuit components. On the contrary, voltage drops across inductances do, because they reach high magnitudes as well as short rise and fall times. Distortions of this kind have the potential of interfering with the operation of integrated circuits and discrete semiconductor devices.

### 10.2.b. Representation in schematics

The schematic of Fig. 19 is abstract, too. However, it shows at its crucial points what requirements should be met by physical connections on the board. This involves the following aspects.

1. Conventionally, diagonal ends of abstract wires indicate the necessity of connecting physical wires, traces or leads directly to the given point.
2. Some wires, although equipotential as abstractions and apparently running (in the schematic) in parallel to each other, cannot be physically connected along their entire length. An example may be the wire leading downwards from the GND pin of the integrated circuit  $U_1$ . Theoretically, it might be directly connected to the wire running at the bottom of the schematic which—as an abstraction—has the same potential (see Fig. 17). However, this bottom wire conducts the load current which has a high value as well as high rise and fall rates when the transistor  $Q_1$  is switching. Thus, a fast varying voltage drop develops across this wire that would interfere with the operation of the integrated circuit, as the potential of the GND pin serves as the reference for all of the internal blocks of  $U_1$ . Any voltage rise or drop at this pin can lead e.g. to an erroneous comparator or latch action.

For the above reasons, the load current should be conducted in a loop separated (along its longest fragment possible) from the integrated circuit power supply loop. The GND pin should therefore not be inserted into the power loop, but directly connected to the capacitor  $C_1$  which stabilises the supply voltage.

### 10.2.c. Specific requirements for connections

Let us now point out the main requirements resulting from the abovementioned issues.

1. To reduce the level of disturbances generated in the high-current loop where high rates of change of currents occur, the associated stray inductance should be minimised. This loop (as marked with circles in Fig. 19) should therefore be the shortest possible.
2. To efficiently protect the drain from a potential rise above that of the positive end of the supply voltage ( $u_i$ ), the terminals of the diode  $D_2$  should be mounted as close as possible to the Q1.D and C1.P pins and any connections involved should be the shortest possible.
3. To effectively carry any disturbance-related charge appearing at the gate off to the power supply ( $u_i$ ) ground, the resistor  $R_5$  should be mounted as close as possible to the gate and source leads of the transistor  $Q_1$ .
4. To reduce the level of disturbances that can be harmful for the transistor's gate circuit and for the integrated circuit, the gate circuit loop (marked with triangles), where a high current flows with high rates of change, too, should have a minimum circumference and a minimum area enclosed, and possibly should have no fragment in common with the power loop. The diagonal line indicates the necessity of connecting U1.GND to Q1.S directly, i.e. of realising a connection that does not have any fragments in common with the power loop or with any other connections to the U1.GND pin.
5. To efficiently carry off any disturbance-related charge and not allow it to penetrate into the integrated circuit, the de-coupling capacitor  $C_3$  should be mounted as close as possible to the U1.VCC and U1.GND pins and any connections involved should be the shortest possible and should be realised without any additional wiring, using just the capacitor's leads.
6. Basically the same applies to the capacitor  $C_4$ , although this one is not as critical as  $C_3$ . To avoid complicating the schematic, the connection of this capacitor has not been marked graphically.
7. To ensure efficient input voltage stabilisation, the capacitor  $C_1$  should be mounted in such a way that the lines in and out are separated, i.e. that the diagonal sections drawn at different angles do not have any fragments in common.
8. To prevent any disturbances coming from the power loop from affecting the power supply of the logic part of the circuit (especially of the integrated circuit), the connections of the U1.VCC and U1.GND pins to the appropriate terminals of the capacitor  $C_1$  should have no fragments in common with the power loop.
9. To minimise the risk of the timer  $U_1$  being interfered, any tracks connected to the fast varying and relatively high potential of the transistor's drain (Q1.D) should not be located in an immediate proximity of this integrated circuit.

The phrase “should not have any fragment in common” must always be understood as aiming towards an ideal. In reality, some common fragment will always exist, should it only be for the component's own leads; it is therefore the minimisation of the length of such a fragment that is aimed at.

The design rules presented and discussed in Section 2.1.b still apply, as well.

### 10.3. Design realisation

#### 10.3.a. Approach and tools

Depending on the team's own skills, the board design may be realised:

- (1) based on the universal prototyping printed circuit board described in Section 10.1.b; you should then follow the general rules presented in Section 2.1.b and the remarks given below;
- (2) as a custom trace layout; in this case, the printed circuit board may be manufactured on your own or at the university using a dedicated milling machine (this requires, however, obeying an additional set of rules as well as considering a realisation time of about one week).

**Custom designs must keep the component designators from Fig. 19.**

To facilitate the realisation and verification of any circuit assembled on the universal board, a component and connection layout of the board should be designed and checked before circuit assembly begins. For this purpose, the worksheet described in Sub-chapter 2.1 is provided which includes a macro for automated design checking.

**Using the worksheet is not imperative. However, the teacher will not help finding errors in designs that have not been checked automatically beforehand.**

The worksheet version for this laboratory contains:

- two sheets named *UM\_8\_10* and *UM\_8\_11*, where images of solder pads and conducting traces of the UM-8 universal board in its 10 and 11-column variants, respectively, have been introduced (Fig. 18, see information in Section 10.1.b),
- a sheet named *Wezły schematu*, where a description of connections between components consistent with the electrical schematic of Fig. 19, has been entered.

There is therefore no need to enter the above data on one's own. Instead, right after opening the worksheet, you should make a copy of the *UM\_8\_10* or the *UM\_8\_11* sheet, according to the board variant used (see Section 10.1.b), and change its name to *Płytką* (exactly this one, with the Polish letter "ł"; you do not have to create the board image as told in the worksheet description).

#### 10.3.b. Physical limitations

Apart from requirements of an electrical origin listed in Section 10.2.c, the existence of a number of mechanical and geometrical limitations must be taken into account. Ignoring them in design may make it difficult or even impossible to commission the assembled circuit or to perform measurements on it. The most important limitations of this kind are as follows.

1. The connectors  $J_1$  and  $J_2$  must be so located and oriented that it is possible to connect wires there. It is therefore best to place them close to board edges. Connector inlets should not be blocked in any way by other components.
2. When the universal board design worksheet is used, sometimes reversing terminal numbering may be profitable for components whose structures are symmetrical. This applies to the connectors  $J_1$  and  $J_2$  as well as the potentiometer  $R_2$ . For this purpose, it is sufficient to change terminal designations inside the appropriate soldering pads in the *Płytką* sheet. It is not possible with other components, because the roles of their terminals are individual and strictly defined; this concerns the transistor  $Q_1$  and the integrated circuit  $U_1$ .
3. The measurement wires  $W_1$ ,  $W_2$  and  $W_3$  should enable a current probe to be connected. Due to the relatively large dimensions of this probe, it may be profitable to place these wires at the bottom side of the board (i.e. on the solder

side instead of on the component side). This will provide a high flexibility as to the placement of their terminals, thus eliminating limitations imposed by other components. These wires do not have to fit inside the board's outline.

4. The measurement point  $P_1$  must enable two voltage probe grounds to be connected in a way ensuring that no undesirable short-circuit is created. It is therefore best to place it at an edge of the board.

The measurement points cannot be placed on the solder side. This is because they are not insulated, while on the solder side, conducting traces and a large number of soldered component leads are located, which might cause random short-circuits.

5. The measurement point  $P_2$  must enable a voltage probe tip to be connected. It must be therefore physically accessible.
6. The possibility of attaching a heat sink to the transistor must be provided. This heat sink would be mounted to the transistor's base while keeping the orientation shown in Table 2. It is therefore profitable to place the transistor close to an edge with its base facing the outside of the board.

### 10.3.c. Design for universal board assembly

When the universal board is used, circuit assembly will be simpler and faster if:

- (1) factory-made traces are used to the maximum extent;
- (2) the number of additional connecting wires is minimised;
- (3) the number of interconnects between neighbouring traces to be realised with solder is minimised, as the board is covered with a mask layer counteracting the formation of such connects, or such connects can be realised by bending a lead of the closest component.



### 11. Required Knowledge

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#### 11.1. Prerequisites

- Principle of switch-mode control and ideal pulse wave parameters (Manual 0, Ref. E; Section 4.2)
- General operating principle of a buck converter (the complete circuit with a transistor, a diode, an inductor and an output capacitor): electrical schematic, switch operation, voltage and current waveforms, ripple factor (Ref. B; Sections 5.2 and 5.3)
- Operating principle of the 555 integrated timer in its astable mode: voltage waveforms, modified configuration (Ref. [19]; Section 6.2)
- MOSFET power loss: instantaneous power in the particular operating states, static and dynamic average power loss (Manual 3P, Refs. A and D; Manual 6P, Refs. A and B)
- Heat conduction: Fourier's law in its simplified form, thermal resistance, equivalent electrical schematic, component cooling using a heat sink (Ref. E)

#### 11.2. Test scope

The problems below concern both Exercises 7K and 3U. The test problem for Exercise 7K will be a computation or design (component selection) one; the problem for Exercise 3U will be a theoretical or experimental (measurement results) one.

1. Switched-mode control: principle, ideal pulse wave parameters. (Manual 0, Ref. E; Section 4.2)
2. Buck converter: schematics (including an abstract switch and including a semiconductor switch), SPDT switch and its operation, role of either passive

component; topology in either sub-interval of the switching period. Inductor, transistor and diode current and voltage waveforms related to the switch control signal, including characteristic values and their relation to circuit operating conditions (load current, input and output voltages, parameters of the pulse wave controlling the transistor: indicating them in plots, without detailed formulae). (Refs. B and C; Sections 5.2 and 5.3; report)

3. Numerical parameters of voltages and currents in a buck converter for its components (inductor, transistor, diode, output capacitor, input capacitor) as well as for the source and the load depending on power supply conditions (input voltage), load conditions (load current) and control conditions (frequency, duty cycle). Computations and their application in component selection using component technical data (knowledge of formulae other than resulting from item 2 is not required as they will be given; selecting a suitable formula and applying it is required) (Ref. B; Sections 5.2, 5.3 and 5.4; report)
4. Voltage conversion ratio: definition, conversion characteristic for an ideal (lossless) buck converter (formula, plot). Average power loss in a MOSFET: static and dynamic components, on-state resistance, effect of temperature. Efficiency: definition, converter power loss formula, effect on voltage conversion ratio. Computations using component technical data and their application in power loss, efficiency and duty cycle prediction. (Ref. B; Section 5.5; Manual 0, Ref. A; Manual 3P, Refs. A and D; Manual 6P, Refs. A and B; report)
5. Fourier's law of heat conduction (practical form as applied in electronic circuit design, simplified approach for high frequencies), junction temperature, thermal resistance (definition, unit). Heat flow path for a semiconductor device cooling system: equivalent electrical circuit: temperatures at characteristic points, thermal resistances for a cooling system with and without a heat sink. Computations using component technical data and their application in thermal safety assessment, thermal safety limits determination and heat sink selection. (Ref. E; report)
6. Thermal breakdown: physical mechanism of thermal instability in a reverse-biased PN junction (in brief, without formulae), practical consequences for device safety; risk level and hazard causes for unipolar (MOSFET) and bipolar (BJT) devices (in brief, without details of physical phenomena). (see Refs. F, G and H)
7. Avalanche breakdown: physical mechanism (in brief, without formulae), practical consequences for device safety. (see Ref. G [14], Section 1.2.7; Manual 0, Ref. L, Section 2.1.3)

When results included in your report are concerned, restrict to the qualitative aspect (mutual relationships and variation nature) disregarding the quantitative one (specific numerical values).

## 12. References

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