Lodz University of Technology
Department of Microelectronics and Computer Science
PL-90924 Lodz, ul. Wolczanska 221/223, bldg. B18
ph. +48 42 631 26 28   fax +48 42 636 03 27   e-mail secretary@dmcs.p.lodz.pl
http://www.dmcs.p.lodz.pl

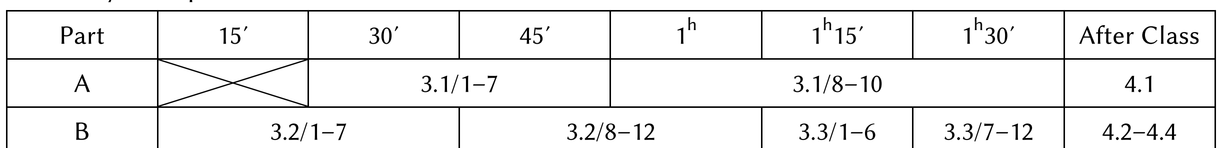
POWER DEVICES AND SYSTEMS LABORATORY

Exercise 1

Diodes

Unipolar and Bipolar Conduction
Voltage Blocking

Indicatory work plan



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Exercise and manual elaborated by
Łukasz Starzak
Part C (ver. 5.2) translated by
Małgorzata Napieralska, Grzegorz Jabłoński

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B

Exercise Introduction

1. Exercise Aim and Plan

The aim of this exercise is to get acquainted with contemporary solutions of power (i.e. high-voltage and high-current) diodes. Nevertheless, conclusions from this exercise may be extended to all the power semiconductor devices. This is because each of them contains in its structure a layer set analogous to one of the analysed diodes. Thus, this exercise constitutes an opportunity to discuss in more detail the idea of semiconductor switch and its properties—both desirable and achievable in reality.

Using simple models implemented in a spreadsheet, an SBD (Schottky) and a PIN power diode will be analysed. The effect of semiconductor structure technological parameters on electrical properties of the analysed devices (considered as switches) will be determined. Putting it more precisely, we will only consider parameters of the lightly doped layer: width and dopant concentration. Blocking and conducting states will be considered separately. Both diodes will be then compared.

For the PIN diode complex dynamic phenomena are typical. To investigate them, additional transient simulations of switching (i.e. turn-on and turn-off) states will be carried out. In this case we will restrain to determining the effect of the most important parameter which is the carrier lifetime.

Using computer models and tools will enable virtual investigation of multiple devices with arbitrarily defined technological parameters in a short time. It is obvious that carrying out an analogous physical experiment would be impossible.

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2. Power Diodes

2.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
A	Ben	5, 5.1	2.1.a—b; #0 6.2.d, 6.5, 6.6		
B	Ben	5.2	2.1.c; #0 5.2.e, 5.3.b, e—f		
C	Ben	5.3, 5.3.1, 5.3.2	2.2; #0 6.7.b		
D	Ben	5.4	2.3; #0 5.4.c, 6.1.e, 6.7.a		
E	Ben	5.5, 5.5.1, 5.5.2	2.4.a		
F	Moh	20-3, 20-3-1, 20-3-2	2.1.c; #0 5.2.c—f, 5.3.a—b, e—f		3.2
G	Moh	20-4-2	#0 6.1.e		

Additionally, from Manual 0 references:

0 H	Ben	3.1.1	2.1.a, 2.3.a		

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C

Experiment

3. Simulations

3.1. Investigation of PIN and SBD diodes in forward conducting state

Electric potential distribution

This part of exercise should be carried out using the worksheet *pin_sbd_stan_przewodzenia.ods*, which should be copied to the team's account.

The worksheet contains one spreadsheet where three distributions along the x axis, i.e., along the anode to cathode line, are plotted for two power diodes, a PIN and an SBD (Schottky) one:

- $p(x)$, hole concentration distribution,
- $n(x)$, electron concentration distribution,
- $V(x)$, electric potential distribution assuming that the potential of the negative electrode, i.e., the cathode, is zero.

The first two distributions demonstrate what is the concentration of carriers of a given type (i.e., how many of them are contained in a unit volume) at a given distance x from the anode.

The latter distribution shows the **electric potential of a given point relatively to the zero electric potential point**. (Remind that a electric potential value is always relative and depends on which point we assume to have the potential of zero.) As indicated above, in the considered case the lowest potential within the diode, i.e., one of the cathode, is assumed to be zero.

Moreover, electric potential difference between any two points equals the voltage between these points:

$$V(x_2) - V(x_1) = U_{21} \qquad (3.1)$$

Therefore, the **difference between the values of V(x) read out at both ends of a given region** (e.g., emitter layer, charge storage region, junction etc.) tells us how large a **voltage drop is induced across this region by the flowing current**. In the extreme case, the difference between the anode potential and the cathode potential, i.e., the difference between the values at the left and right ends of the curve is equal to the total voltage drop across the diode in the conducting state.

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Observation of the $V(x)$ distribution allows us to determine:

1° what the **total voltage drop** U_F across a diode with given parameters and under given current density is: according to the above ($V_K = 0$), it equals the anode electric potential V_A;

2° what the **contributions of the particular components** (see Refs. A and D) are to this total voltage drop.

Additionally, the shape of the distribution curve in a given layer indicates the **character of conductivity**. In layers exhibiting unipolar (drift) conductivity, the resistivity $\rho(x)$ is constant, so across every elementary section Δx the same voltage will be dropped, equal

$$\Delta U = \rho(x) \cdot \Delta x \cdot J \tag{3.2}$$

which implies the linear character of the electric potential distribution curve.

On the other hand, in layers exhibiting bipolar conductivity (drift and diffusion), the resistivity $\rho(x)$ at every point of the lightly doped layer depends on the concentration of excess carriers at this point. As this concentration varies along the x axis then according to the above equation, across different elementary sections Δx we will observe different elementary voltage drops. Thus in this case, the character of the electric potential distribution curve will be non-linear.

Using the spreadsheet

The distributions plotted in the spreadsheet depend on the following parameters visible in the window:

(1) general constants and physical parameters:
- e – electric charge of the electron,
- μ_n and μ_p – electron and hole mobilities,
- n_i – intrinsic semiconductor equilibrium carrier concentration,
- k – Boltzmann constant,
- D_n, D_p, D_a – electron, hole and ambipolar diffusion constants,
- A^* – Richardson constant;

(2) technological parameters of the device:
- **N_D – dopant concentration in the lightly doped layer,**
- **W_I – lightly doped layer width,**
- **τ – minority carrier lifetime in the lightly doped layer (only applicable to the PIN diode),**
- A – the cross-section perpendicular to the anode-cathode axis,
- N_{D+} and W_{N+} – dopant concentration and the width of the N^+ layer (W_{EN} or W_{SN}), respectively
- N_{A+} and W_{P+} – dopant concentration and the width of the P^+ layer (only for the PIN diode),
- φ_B – the potential of the energy barrier in the Schottky junction (only for the SBD diode),
- N_{Al} and t_M – electron concentration for aluminium and the thickness of the metal electrode (only for the SBD diode);

(3) device operating conditions which in case of the forward conducting state can be limited to:
- **I_F – current forced through the structure.**

Parameters intended to be changed by the student have been marked above and in the spreadsheet in bold type. The remaining parameters should not be changed. It is best to confirm a new value with *Alt+Enter* because the cursor will not move to the next cell then.

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To avoid obscuring the picture of phenomena and allow the most thorough observation possible of the key lightly doped N^- layer, the distributions are plotted with the assumption of the abrupt character of the junctions, i.e., the voltage drop across the junction occurs at an infinitely small distance Δx. Moreover, the heavily doped N^+ layer can be shown cut from its right-hand side to avoid the inconvenient change of scale of the x axis (which would make a precise distribution analysis in the N^- layer impossible).

To facilitate the analysis of the total voltage drop across the diode as well as of the contributions of its individual components, the spreadsheet computes and displays:

- the total voltage drop across the diode U_F,
- voltage drop components of the SBD diode:
  - U_M, across the metal electrode,
  - U_J, across the metal-semiconductor (Schottky) junction,
  - U_I, across the lightly doped layer and
  - U_S, across the N^+ substrate;
- voltage drop components of the PIN diode:
  - U_{EP}, across the P^+ emitter,
  - U_{JP}, across the P^+N^- junction,
  - U_I, across the lightly doped layer,
  - U_{JN}, across the N^-N^+ junction and
  - U_{EN}, across the N^+ emitter.
- the resistance of the lightly doped layer R_I.

Saving results

Performing tasks should be documented by saving the obtained graphs together with parameter values for which they have been obtained. For this purpose you must use the *Kopiuj/Copy* button, which copies the appropriate spreadsheet fragment to the clipboard.

For the *Kopiuj/Copy* button to work correctly, the spreadsheet window must be the active one.

For the *Kopiuj/Copy* button to work, macros must first be enabled, which are disabled by default in the LibreOffice package. This can be done from the menu *Tools* > *Options* > *LibreOffice* > *Security* > *Macro Security*; set security level to *Low*. After this change is made, close and reopen the worksheet.

The fastest and the most reliable way to save the copied spreadsheet contents is to paste it to a LibreOffice text document in the following way:

- from the menu choose *Edit* ▸ *Paste special* or press *Ctrl+Shift+V*;
- choose the *Bitmap* option and accept the choice;
- click with the right mouse button on the pasted drawing;
- from the context menu choose *Anchor* ▸ *As character*;
- insert a new line after the picture (*Enter*).

The influence of the basic technological parameters on the voltage drop

1. Enter your team number and academic year into the appropriate spreadsheet fields.

   Submitting results without the above fields filled in will be considered as cheated.

2. From the web page, obtain and enter into the appropriate field the initial dopant concentration in the lightly doped layer $N_{D,ini}$.

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3. Determine a set of three values of N_D for which the virtual experiment will be performed. For this purpose, multiply or divide the value of $N_{D,ini}$ determined in step 2 by the successive powers of 10 so as to obtain one value for each of the orders of: 10^{13}, 10^{14} and 10^{15} cm^{-3}.
4. From the web page, obtain and enter into the appropriate field the initial width of the lightly doped layer $W_{I,ini(A)}$.
5. Determine a set of three values of W_I for which the virtual experiment will be performed: $\{W_{I,ini(A)}/3;\ W_{I,ini(A)};\ W_{I,ini(A)}\times 3\}$.
6. From the web page, obtain and enter into the appropriate field the initial value of the minority carrier lifetime for the PIN diode τ_{ini}.
7. Ensure that: $N_D = N_{D,ini}$, $W_I = W_{I,ini(A)}$, $\tau = \tau_{ini}$ in the spreadsheet. For three current values $I_F = \{1; 10; 100\}$ A:
   (a) write down (or copy to a separate sheet) the parameters of: N_D, W_I, τ, I_F, and voltage drops U_F across SBD and PIN diodes;
   (b) save the graphs together with parameter values in the way indicated above.
8. Keep: $W_I = W_{I,ini(A)}$, $\tau = \tau_{ini}$. For the 2 remaining values of N_D determined above (i.e., excluding $N_{D,ini}$), for three current values $I_F = \{1; 10; 100\}$ A (e.g., six combinations of N_D and I_F in total at constant W_I and τ):
   (a) write down the parameters of: N_D, W_I, τ, I_F, and voltage drops U_F across SBD and PIN diodes;
   (b) save the graphs together with parameter values.
9. In the appropriate spreadsheet cells, enter: $W_I = W_{I,ini(A)}$, $\tau = \tau_{ini}$. For the 2 remaining values of W_I determined above (i.e. apart from $W_{I,ini(A)}$), for the 3 values of the current $I_F = \{1; 10; 100\}$ A (i.e. for the 6 combinations of W_I and I_F with N_D and τ kept constant):
   (a) write down the parameters of: N_D, W_I, τ, I_F, and voltage drops U_F across SBD and PIN diodes;
   (b) save the graphs together with parameter values.

Influence of the minority carrier lifetime in the PIN diode

10. In the appropriate spreadsheet cells, enter: $W_I = W_{I,ini(A)}$, $I_F = 10$ A; keep $N_D = N_{D,ini}$, $\tau = \tau_{ini}$. Starting with this case:
    (a) save the worksheet;

    The worksheet should not be saved (unless under a different file name) after the following sub-steps of this step are carried out. If a need to repeat earlier steps occurs after they are realised, close the worksheet, then re-open the file saved in the above sub-step. Otherwise, graph scales will differ which will make them impossible to compare.

    (b) zoom the carrier concentration axis for the PIN diode:
    - double-click the PIN diode graph,
    - in the drop-down list in the upper toolbar choose *Y Axis* and click the *Format Selection* button beside,
    - enter 10^{12} (using the "1E12" notation) as the minimum value and 10^{18} ("1E18") as the maximum one and accept,
    - terminate graph edition by clicking in the spreadsheet outside the graph's area;

    (c) write down the values of: N_D, W_I, τ, I_F, and the voltage drop U_F across the PIN diode (without considering the SBD);
    (d) save the graphs together with parameter values;
    (e) reduce the excess carrier lifetime to $\tau = \tau_{ini}/3$ and repeat sub-steps (c)–(d).

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3.2. Investigation of the PIN diode in reverse blocking state

Using the spreadsheet

This part of exercise should be carried out using the worksheet *pin_stan_zaworowy.ods*, which should be copied to the team's account.

The worksheet contains one spreadsheet, displaying the electric field distribution $E(x)$ along the PIN ($P^+N^-N^+$) diode. The word "distribution" means a graph showing values of a given physical quantity in various points of the space. In the considered, simplified case the space is one-dimensional: it is limited to the *x*-axis which is identified as the anode-cathode line (see Ref. B, Fig. 5.7). Thus, the distribution curve $E(x)$ shows how strong electric field is at a given point of the diode (defined by the distance *x* from this point to the anode).

The electric field distribution in the given semiconductor structure depends on the following parameters visible in the spreadsheet window:

(1) general constants and physical parameters, such as:
- e – electric charge of an electron,
- ε_{Si} – relative permittivity of silicon,
- ε_0 – absolute permittivity of vacuum,

(2) technological parameters of the device, namely:
- **N_D – dopant concentration in the lightly doped layer,**
- **W_I – width of the lightly doped layer (base),**
- N_{D+} – dopant concentration in the emitter layer N^+,
- N_{A+} – dopant concentration in the emitter layer P^+;

2) device operating conditions which in the case of reverse bias can be limited to:
- **U_R – reverse bias voltage applied across the structure.**

The parameters intended to be changed by the student are marked above and in the spreadsheet by the bold font. The remaining parameters should not be changed. It is best to confirm the new value by using the key combination *Alt+Enter* because the cursor will not move to the next cell then.

To facilitate determination if avalanche breakdown or punch through occurs in the structure, there are two lines visible in the graph:
- E_{crit} – indicating the level of the critical electric field,
- W_I – indicating the end of the lightly doped layer.

Additionally, below the U_R value there is a field where one of the following messages is displayed:
- *Applied* – if the entered voltage value can appear across the device,
- *Impossible* – if it is not physically possible for the entered value voltage to appear across the device because at a lower voltage the device would already enter breakdown state, which would make it conduct a very high current that would cause opening of the circuit due to one of its elements breaking down.

Based on the input parameters, not only the field distribution is drawn, but also the following values are computed:
- the critical electric field E_{crit},
- maximum electric field along the *x* axis E_{max},
- the width of the space charge regions in the subsequent layers – $W_{sc(P+)}$, $W_{sc(N-)}$ and $W_{sc(N+)}$.

Performing tasks should be documented by saving the obtained graphs together with parameter values for which they have been obtained (still using the *Kopiuj/Copy* button). To accomplish this

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you should proceed as in section 3.1. Saving graphs for both diodes at the same time (which is possible using the *Copy/Paste* button) will make their later comparison easier.

Depending on parameter values, the displayed structure may represent a device with or without punch through. These are often referred to as non-punch-through (NPT) and punch-through (PT) devices, respectively. However, another classification defines punch-through devices as *invulnerable to punch through*, and not those with *punch through occurring* during their operation. These two approaches can give equivalent results but this is not always the case. For example, the PIN diode is invulnerable to punch through by its semiconductor structure but it can be manufactured as a wide-base device where punch through does not have any possibility to occur; depending on the definition chosen, such a device can be classified as NPT or as PT. Therefore, to avoid misunderstanding, we will not use the common abbreviations NPT and PT, with the exception of symbol subscripts. Instead, we will refer to the analysed structures as to “without punch through” and “with punch through” meaning “where punch through occurs during operation” and “where punch through does not occur during operation.”

Devices without punch through

1. Put the group number and the academic year into the appropriate field of the spreadsheet.

   Submitting of the results without the above fields filled correctly will be considered as cheating.

2. Put into the appropriate field the initial dopant concentration $N_{D,ini}$ as determined in step 3.1/2.
3. From the web page, obtain and enter into the appropriate field a new initial width of the lightly doped layer $W_{I,ini(B)}$.
4. For the current parameters of the semiconductor structure:
   (a) by experimentally changing the value of the reverse bias voltage U_R and observing the maximum value of the electric field, determine (with an accuracy of 1 to 5%) the avalanche breakdown voltage U_{br};
   (b) based on the electric field distribution being observed, determine the type of the diode with the current parameters: with or without punch through;
   (c) write down (or copy to the separate sheet) the following parameters: N_D, W_I, U_{br} and the diode type;

      In case of copying, obligatory use the function *Paste Special* and uncheck the *Formulas* field.

   (d) save the graph together with the parameter values in the way described above.
5. Repeat the entire step 4 for each of the further cases obtained by successive division of the value of W_I by 2, e.g. for $W_I = W_{I,ini(B)}$ / {2; 4; 8; ...} down to the value, for which the diode becomes a device with punch through; for this last case, skip sub-steps (c)—(d).
6. Determine the minimum base width $W_{I,npr,min}$ for a diode without punch through:
   (a) by alternately changing the values of U_R and W_I obtain at the same time:
      - the voltage for which the diode will be at the boundary of avalanche breakdown (the electric field distribution at its maximum value E_{max} will be useful) and
      - such a base width that its further shortening would cause the diode type to become one with punch through (the electric field distribution and the width of the space charge in the N^+ layer $W_{sc(N+)}$ will be useful);
   (b) write down the parameters: N_D, $W_I = W_{I,npt,min}$, U_{br};
   (c) save the graph together with the parameter values.
7. Starting from the case obtained in the previous step, investigate the influence of the dopant concentration in the lightly doped layer:
   (a) change the dopant concentration N_D to $N_{D,ini}/2$ and repeat step 6;
   (b) change the dopant concentration N_D to $2{\times}N_{D,ini}$ and repeat step 6;

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Devices with punch through

8. Restore the dopant concentration of $N_{D,ini}$. Decrease the width of the lightly doped layer to $W_{I,ini(B)}/200$ ($\underline{W_{I,ini(B)}}$, not the current value of W_I nor $W_{I,ini(A)}$).
9. Repeat step 4 for the new base width.
10. Repeat the <u>entire</u> step 4 for <u>each of</u> the cases obtained by successive multiplication of W_I by 2, i.e. for $W_I = (W_{I,ini(B)}/200)\times\{2, 4, 8, \ldots\}$. Repeat the procedure <u>while</u> the base width is <u>lower</u> that the limit value found in point 6.
11. For $W_I = (W_{I,ini(B)}/200)\times 4 = W_{I,ini(B)}/50$:
    (a) by changing the value of the reverse bias voltage U_R, observing the electric field distribution and the width of the space charge in the N^+ layer, experimentally determine the value of the punch-through voltage U_{pt};
    (b) save the graph together with the parameter values.
12. Leave $W_I = (W_{I,ini(B)}/200)\times 4 = W_{I,ini(B)}/50$. Investigate the influence of dopant concentration in the lightly doped layer:
    (a) change the dopant concentration N_D to $N_{D,ini}/2$ and repeat step 4;
    (b) change the dopant concentration N_D to $2\times N_{D,ini}$ and repeat step 4.

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3.3. Investigation of PIN diode switching

Using the electronic circuit simulator

To investigate the dynamic processes taking place during PIN diode turn-on and turn-off, the DMCS-SPICE environment with a physical model of this device implemented will be used. Its kernel is based on the Spice 3f5 simulator, the latest version of the original simulator written at the University of California, Berkeley (USA). The Spice program became the basis for many popular electronic circuit simulators such as PSpice used in Exercise 6[A].

The main simulator window allows entering circuit description or loading it together with simulation settings. Simulation is run with the *Simulate* button. When it completes, its results are displayed in the same window. The *Back to netlist* button allows returning to the circuit description page (the browser's *Back* button should not be used for this purpose).

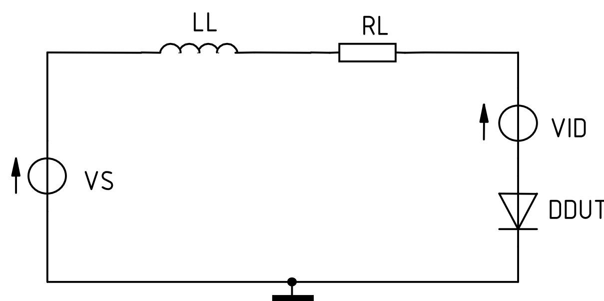

Fig. 1. Circuit schematic for simulation of PIN diode switching

The simulations should be performed for the circuit containing an inductance, depicted in Fig. 1. Its description will be loaded to the simulator at the appropriate moment. The circuit operates as follows. The voltage across the source V_s changes from 100 V to −100 V at the time moment t = 10 µs, and subsequently back to 100 V at the time moment t = 40 µs. The load has the parameters of: R_L = 10 Ω, L_L = 100 µH. For all the teams, the investigated device will be the diode D_{DUT} with the parameters of: $N_D = 1{\cdot}10^{14}$ cm^{-3}, W_I = 200 µm, τ = 10 µs. The additional zero voltage source V_{ID} connected in series with the diode is used to measure its current. This is due to the limitation of the Spice version used by the simulator, which does not allow measuring diode currents directly.

Dynamic operating states of the PIN diode

1. In the web browser, open the DMCS-SPICE web page by entering the address given above.
2. Click *Load circuit* and load the circuit description from the file *pin_przelaczanie.dsc.*
3. Run simulation with the *Simulate* button. A graph containing the following waveforms should appear on the result presentation page:
    - V(1), V_s source voltage,
    - I(VID), current through the diode D_{DUT},
    - V(4), voltage across the diode D_{DUT}.

    Use the *Refresh plot* button to update the graph after a possible change in axis description, axis range or after enabling logarithmic scale.

4. In the *Advanced Results* pane, select the *DDUT* diode on the *Carrier concentration and electric potential* list and click *Load.* This will open a new window containing the waveforms of diode current and voltage.
5. In the *Graph Title* field enter your team number, which should appear as the title of all saved graphs.

    Use the *Refresh plot* button to update the graph after a change in the title or axis range.

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Plots without team number will be considered as cheated.

6. Observe and save the current and voltage waveforms.

   Graphs are normal pictures that can be saved on the computer as separate files or copied and pasted to a LibreOffice text document.

7. * Based on the diode current waveform, determine time intervals where this devices operates in the forward conducting (on), turn-off, reverse blocking (off) and turn-on states. Make use of the axis scale change function to take a closer look at the voltage waveform also in those states where it seems to have a constant value of zero (which is not true, but this can only be seen after zooming in). Save any plots that show features invisible in the plot saved in step 6.
8. * Click on the diode current waveform within the forward conduction interval. A new window will open, containing carrier concentration distribution $p(x)$ in the diode base at the chosen time instant at the top and electric potential distribution $v(x)$ at the bottom. The x-axis is defined as in the spreadsheet, while the distributions depict only the range of $0 \le x \le W_I$, i.e., only the lightly doped layer (including the voltage drops on junctions which can be seen at the very edges).

   If in the browser a message about pop-up blocking appears, you must allow pop-ups from the oracle.dmcs.p.lodz.pl domain and then click on the graph again.

   To obtain distributions for a different time moment in the future, it is not necessary to close the window. It is enough to activate the previous one (with diode voltage and current waveforms) and click on the graph at a different point. The distributions window will be re-activated and its contents updated.

9. * Obtain and save the distributions of carrier concentration and electric potential in the diode base for various time instants. Choose the instants reasonably in a way that the series of graphs obtained illustrates phenomena occurring in all the four operating states of the diode: two static and two dynamic ones.

   Tracking the carrier concentration variation will be easier if a constant (not automatic) range of the carrier concentration axis is chosen, or at least the lower bound of this range is set to zero.

10. Limit the simulation time (the *STOP* field) to 30 μs.
11. Observe the changes in circuit waveforms (voltage and current) occurring as a result of threefold decrease in the carrier lifetime τ:
    (a) change accordingly the value of the *L2_TAU0* parameter in the DMOD diode model in the *Circuit Description* field;
    (b) write down both values of carrier lifetime (the initial and the modified one);
    (c) run simulation;
    (d) save diode voltage and current waveforms.
12. End the simulator session by pressing *End session* in its main window.

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D

Results

4. Results Processing and Analysis

4.1. Conducting state

Carrier concentration distribution

1. Fill in Section 1 of the report.

Electric potential distribution

2. Fill in Section 2 of the report.

Components of the total voltage drop

3. Fill in Section 3 of the report.

Static characteristics against current

4. In the table in Section 4 of the report, gather numerical results obtained for conducting state at a constant minority carrier lifetime $\tau = \tau_{ini}$ (Section 3.1 except point 10):
   - dopant concentration in the lightly doped layer N_D,
   - lightly doped layer width W_I,
   - forward current I_F,
   - voltage drop across the structure U_F.

   Leave R_{on} and P_{on} columns unfilled for now.
5. Complete the table by calculating (based on results previously stored there) for each of the diodes:
   (a) the equivalent on-state resistance

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$$R_{\text{on}} = \frac{U_{\text{F}}}{I_{\text{F}}} \tag{4.1}$$

(b) average on-state power loss

$$P_{\text{on}} = I_{\text{F}} U_{\text{F}} \tag{4.2}$$

All the investigated cases will be analysed. Even a superficial analysis of the results shows that some of them cannot occur in practice, e.g. a power loss of the order of 10 kW in a single semiconductor device would cause its immediate destruction. This demonstrates the usefulness of simulation which helps the circuit engineer understand why devices of certain parameters are not manufactured whereas they allow the device designer to reject some solutions in advance without the need for physical testing.

6. Obtain and embed in the report plots of voltage across the diode U_{F}, equivalent resistance R_{on} and power dissipation P_{on} as functions of forward current, for 3 different dopant concentrations in the lightly doped layer N_{D}:
   (a) from the table, select data obtained for the same lightly doped layer width $W_{\text{I}} = W_{\text{I,ini(A)}}$, but for three different dopant concentrations N_{D};
   (b) based on the selected data, draw a family of voltage characteristics $U_{\text{F}} = f(I_{\text{F}})$ for two diodes and three values of N_{D} (a total of six curves);
   (c) change the scale of both axes to logarithmic (LibreOffice: double-click on the axis and select *Logarithmic scale* in the *Scale* tab);
   (d) display the minor grid (LibreOffice: from the menu, select *Insert* ▸ *Grid* and check the appropriate boxes);
   (e) for each of the six curves, add power trend lines, i.e. of the form of $y = bx^a$ (LibreOffice: select the curve with the mouse or select from the drop-down list in the toolbar, select *Insert* ▸ *Trend Lines* from the menu, select the appropriate regression type and check *Show Equation*);

   The amount of space occupied by the line equation can be reduced by applying an appropriate number format (decimal place count; LibreOffice: double-click on the equation).

   (f) similarly, plot the characteristics of $R_{\text{on}} = f(I_{\text{F}})$ and $P_{\text{n}} = f(I_{\text{F}})$.
7. Complete Section 4 of the report.

Effect of structure parameters

8. By analogy to point 6, obtain and embed in Section 5 of the report plots of voltage across the diode U_{F}, equivalent resistance R_{on} and power dissipation P_{on} against forward current, for three different lightly doped layer widths W_{I} and the same dopant concentration $N_{\text{D}} = N_{\text{D,ini}}$. Do not add trend lines in this case.
9. Complete Section 5 of the report.

Current capability

10. Determine the current capability of the analyzed diodes:

    Current capability is not a universal parameter but one closely related to the thermal properties of the specific structure, its specific housing and a specific associated cooling system. To determine current capability, it is therefore necessary to make an assumption as to a specific maximum power that can be conducted out the hypothetical device. One should be aware that under different assumptions, results would be quantitatively (but not qualitatively) different.

    (a) from the website, obtain the maximum admissible power dissipation in the diode $P_{\text{d,max}}$ to be assumed;

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(b) from the plots of $P_{on} = f(I_F, N_D)$ and $P_{on} = f(I_F, W_I)$ for the SBD and PIN diodes with different technological parameters of N_D and W_I (a total of ten devices), read out the maximum admissible forward current I_{Fmax}, i.e. the forward current value I_F (the x-coordinate), for which the power dissipated P_{on} equals the assumed admissible power $P_{d,max}$ (the y-coordinate);

Use the minor grid of the graph and perform the read-out with a precision achievable with its help (at least 0.5 division).

For a better understanding of the I_{Fmax} read-out method, it may be helpful to analyse the example graph together with the values read out from it included in the report template.

(c) collect your results in the table in Section 6 of the report.

11. Based on appropprately selected rows of the table, plot and embed in the report the relationships of $I_{Fmax} = f(N_D)$ and $I_{Fmax} = f(W_I)$ for both diode types. Apply logarithmic scale to both axes.
12. Complete Section 6 of the report.

Effect of minority carrier lifetime (PIN diode)

13. Fill out Section 7 of the report.

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4.2. Blocking state

Electric field distribution

1. In Section 1 of the report, place the saved graphs of electric field distribution, appropriately grouped.
2. Complete Section 1 of the report.

Effect of the lightly doped layer width on voltage capability

3. Collect the numerical results written down in the table in Section 2 of the report. Place breakdown voltages in separate columns for structures without and with punch through. The diode without punch through of the minimum width $W_{\mathrm{I,npt,min}}$ is a limit case and should therefore be included in both columns.
4. Complete Section 2 of the report.

Effect of the lightly doped layer doping on voltage capability

5. Fill in Section 3 of the report.

Breakdown voltage for structures without and with punch through

6. Fill in Section 4 of the report.

Evaluation of different device types in terms of their capabilities

7. Fill in Section 5 of the report.

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4.3. Switching

Effect of minority carrier lifetime on dynamic properties

1. In Section 6 of the report, embed the saved graphs of PIN diode current and voltage waveforms during switching for two lifetime values.
2. Complete Section 6 of the report.

Physical phenomena during switching

3. * In the appropriate space in Section 7 of the report, assemble plots of carrier concentration and electric potential distribution in the lightly doped layer of the PIN diode saved for subsequent instants. Graphs must be arranged chronologically, with corresponding graphs for the same instant must be placed one next to another. Label graphs for successive instants with letters. In the figure label, name the operating states of the diode corresponding to each of these instants.
4. * In the current and voltage waveforms graph for the initial minority carrier lifetime (as in point 1), mark and label (in the same way as in point 3) time points for which distribution graphs have been saved. Embed the modified graph in the report.
5. * Embed in the report the zoomed graphs showing features invisible in the graph that covers the entire switching cycle. In the figure label, name the corresponding operating states of the diode.
6. * Complete Section 7 of the report.

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4.4. Alternative parameters of diodes with a specified voltage capability

1. * Let us assume that it is possible to manufacture a diode with an epitaxial lightly doped layer of a precisely set dopant concentration equal to $N_{D,ini}/5$. As a result, instead of the diode without punch through having the doping of $N_{D,ini}$ and the minimum layer width $W_{I,npt,min}$, a diode with punch through can be realised still exhibiting the same voltage capability U_{br}. Use the spreadsheet for blocking state investigation, determine the technological parameters for the latter device:
   (a) in the appropriate cells, enter: $N_D = N_{D,ini}$, $W_I = W_{I,npt,min}$;
   (b) from the results table, read out the avalanche breakdown voltage U_{br} for the diode with the above parameters and enter into the spreadsheet as the reverse voltage U_R;
   (c) make sure that the electric field distribution shows the case of the minimum lightly doped layer width for a diode without punch through;
   (d) by changing the lightly doped layer width, determine and write down its specific value $W_{I,pt}$ for which voltage capability returns to the value read out in point (b);
   (e) embed the graph together with parameter values in Section 8 of the report.
2. * Use again the spreadsheet for conducting state investigation to determine the voltage drop across the PIN diode without punch through ($N_{D,ini}$, $W_{I,npt,min}$):
   (a) from the website, obtain and write down the initial value of the minority carrier lifetime for this task $\tau_{ini(B)}$;
   (b) in the appropriate spreadsheet cells, enter: $N_D = N_{D,ini}$, $W_I = W_{I,npt,min}$, $\tau = \tau_{ini(B)}$ (τ, not τ_{ini} of Section 3.1);
   (c) from the results table found in Report 1A (Part 6), read out the maximum admissible forward current I_{Fmax} for the PIN diode with the doping of $N_{D,ini}$ and enter into the spreadsheet as the forward current I_F;
   (d) write down the forward voltage U_F of the PIN diode obtained in this way;
   (e) embed the graph together with parameter values in Section 8 of the report.
3. * Determine the voltage drop across the PIN diode with punch through exhibiting the same voltage capability, which has been obtained in point 1, keeping the minority carrier lifetime unchanged (diode with punch through, option 1):
   (a) change the parameters of the lightly doped layer for ones determined in point 1, i.e. $N_D = N_{D,ini} / 5$ and $W_I = W_{I,pt}$, while leaving $\tau = \tau_{ini(B)}$;
   (b) write down the forward voltage U_F of the PIN diode obtained in this way;
   (c) embed the graph together with parameter values in Section 8 of the report.
4. * Obtain an alternative structure of the diode with punch through: exhibiting an identical forward voltage as the diode without punch through (diode with punch through, option 2):
   (a) experimentally shorten the minority carrier lifetime τ so that the U_F voltage of the PIN diode was the same (with an accuracy of ±0.002 V; it may be necessary to enter the value of τ with an accuracy of 0.001 µs) as for the diode without punch through (point 2);
   (b) write down the forward voltage U_F of the PIN diode obtained in this way;
   (c) embed the graph together with parameter values in Section 8 of the report.
5. * Collect the numerical results obtained in the table in Section 8 of the report.
6. * Complete Section 8 of the report.

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E

Information

5. Required Knowledge

5.1. Prerequisites

Week one

- Carrier concentration and voltage drop across a semiconductor layer in the case of drift only and in the case of drift and diffusion.
  (see Ref. A and Manual 0, Refs. I and J)
- PIN and SBD diode structures (cross-section).
  (see Man. 0, Ref. H)

Week two

- Electric field distribution at a reverse-biased PN junction. Avalanche breakdown condition. Punch through condition.
  (see Refs. B and F; lecture)
- Voltage and current waveforms during PIN diode reverse recovery. Reverse recovery time.
  (see Ref. C)

5.2. Test scope

Answers to most of the below problems are contained in your report and has already required to refer to the referenced sections of the textbooks. Only for certain problems it may be necessary to study the textbooks once again. As far as numerical results contained in the report are concerned, confine to the qualitative aspect (value in comparison to other cases, relationship character), disregarding the quantitative one (specific absolute values).

1. Unipolar and bipolar conduction; the Schottky diode (SBD) and the PIN diode in their conducting state. SBD and PIN structure cross-section.

   Drift and diffusion: physical mechanisms; current density, conductivity, resistivity, voltage drop (formulae symbols and components explanation, without necessarily knowing these formulae by heart).

   Carrier concentration and electric potential distribution in the lightly doped layer (plots); effect of current density on carrier concentration (value considered globally), with explanation. Effect of current density and of lightly doped layer technological

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parameters (dopant concentration and width) on conductivity, resistivity and voltage drop across this layer, with explanation (relation to carrier concentration).

Conductivity modulation: in which device it occurs, what it consists in, what it results from, what profit it brings. Effect of minority carrier lifetime on carrier concentration and voltage drop for bipolar conduction.

(see report; for SBD and unipolar conduction: Ref. D and Manual 0, Refs. H and I; for PIN diode and bipolar conduction: Ref. A and Manual 0, Refs. H and J)

2. Physical mechanisms during switching of unipolar and of bipolar devices. Consequences for switching times; effect of minority carrier lifetime for a bipolar device.

   (see Refs. C and D; Man. 0, Ref. H; report)

3. High voltage devices in the blocking state.

   Asymmetric PN junction space charge region at reverse bias: electric field distribution (plot). Effect of semiconductor layer parameters (permittivity, dopant concentration)—application of Poisson's law).

   Effect of lightly doped layer thickness (width): structures without and with punch through. Effect of the applied reverse voltage—application of the relationship between voltage and electric field distribution.

   Avalanche breakdown and punch through: physical phenomena, conditions of occurrence. Relation of breakdown voltage to lightly doped layer technological parameters (dopant concentration, width) for structures without and with punch through, with explanation.

   (see report; Refs. B and F , and Man. 0, Refs. K and L)

6. References

Benda V., Gowar J., Grant D. A.: *Power Semiconductor Devices: Theory and Applications.* Wiley, 1999. ISBN 0-471-97644-X.

Mohan N., Undeland T. M., Robbins W. P.: *Power Electronics: Converters, Applications, and Design.* 3rd Ed. Wiley, 2003. ISBN 0-471-22693-9.

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