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POWER DEVICES AND SYSTEMS LABORATORY

Exercise 3^{B}

MOSFETs

Buck converter
Pulse width modulation

Indicatory work plan

15′	30′	45′	1^{h}	1^{h}15′	1^{h}30′	After Class
4.2	4.3/1–9	4.3/10–14	4.3/15–20	4.4/1–5	4.4/6–13	5

To be executed before class: 4.2/9(b), 4.3/2(c)

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Parts C and D based on translation of ver. 5.4 by
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Łódź 2015

ver. 6.6.5 (en). 23/10/2015

Contents

B

Exercise Introduction

1. Exercise Aim and Plan

The purpose of this part of the present exercise is to investigate the operation of a MOSFET in its typical application, which is a DC/DC converter. In this circuit, the transistor is a component of a single-pole double-throw (SPDT) semiconductor switch whose role is to switch over a current from one branch to another one. The converter example enables to get acquainted with the pulse width modulation (PWM) method of controlling power semiconductor devices.

This exercise demonstrates that the switched-mode technique using power transistors enables to accomplish useful functions in DC circuits together with achieving high energy conversion efficiency. As always, this has some limitations, introduced in a great part by the semiconductor switch itself. At the end, its properties will be related to those of the complete converter.

2. DC/DC Converters

2.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
A	Ben	4.5	2.1.a—b		

Additionally, from Manual 0 references:

0 B	Eri	1.1	2.1.b, 2.2a—b, 2.3.a,c,d, 3.1.a—b		
0 E	Ras	6.2	2.2, 2.3.a—c		2.2

2.2. Switch-mode control

Obtaining the switch-mode operation of a converter circuit requires switch-mode control of semiconductor devices instead of continuous (linear) control. A controlling quantity x (current or voltage) then takes the form of a pulse wave. It consists of periodically repeated pulses, i.e. sections of a level higher than the idle one, whose shape, to simplify, can be considered rectangular [see Fig. 1(a)].

A pulse wave is described by the following parameters:

(1) ***period of repetition*** T_p which is of course the shortest time after which the waveform repeats, so e.g. the interval between the beginnings of successive pulses;

(2) ***frequency of repetition*** f_p which is the inverse of the period of repetition

$$f_\mathrm{p} = \frac{1}{T_\mathrm{p}} \tag{2.1}$$

(3) ***pulse width*** t_p which is the duration of the top of the pulse;

(4) ***duty cycle*** (also called *duty ratio*) D which is the ratio of the pulse width of the period of repetition:

$$D \overset{\Delta}{=} \frac{t_\mathrm{p}}{T_\mathrm{p}} \tag{2.2}$$

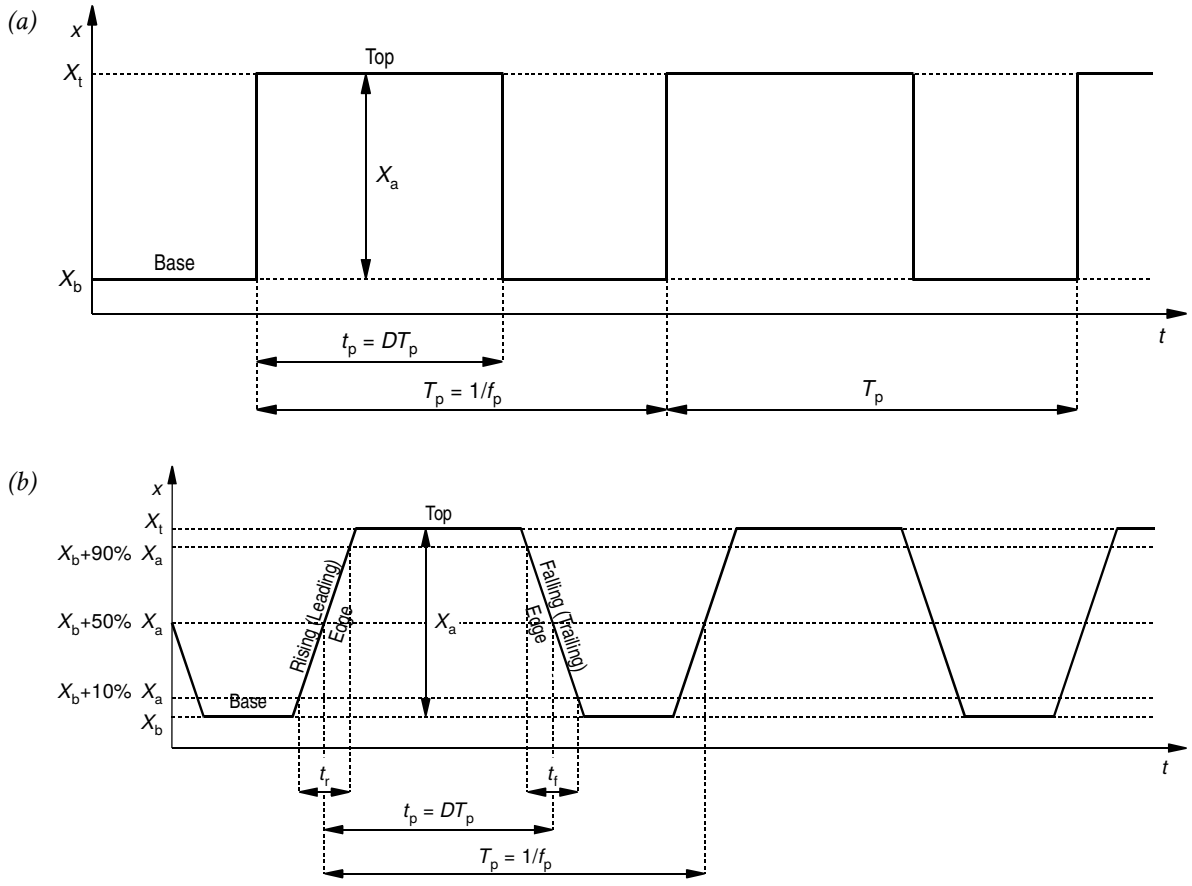

Fig. 1. Pulse wave and its basic parameters: (a) the ideal waveform; (b) a waveform with finite edge steepness

As it can be easily seen, just one of the parameters 1 or 2 and one of the parameters 3 or 4 are sufficient for an unambiguous description of a pulse wave in the time domain.

In the domain of the given electrical quantity (current or voltage), a pulse wave is described by:

(5) ***low level*** X_L which is the value of x corresponding to the base of the pulse;

(6) ***high level*** X_H which is the value of x corresponding to the top of the pulse;

(7) ***amplitude*** X_m which is the distance between the low and the high levels

$$X_m = X_H - X_L \tag{2.3}$$

As it can be seen, any two of the parameters 5 to 7 are sufficient for an unambiguous description of a pulse wave.

In power electronics, very often waveforms with a zero base level ($X_L = 0$) are met, for which $X_H = X_m$. Because of the prevalence of this case and due to the considerable simplification of relationships that are obtained, it is usually the zero base level that is assumed in analysis.

The above mentioned parameters fully describe only ideal pulses. In power electronics, it is the non-zero edge duration that is the most often considered feature of a real pulse wave. These edges are described by [see Fig. 1(b)]:

(8) ***rise time*** t_r, i.e. the time it takes for the waveform to rise from 10% to 90% of its amplitude, which is a measure of the duration of the rising edge (also called the leading edge);

(9) ***fall time*** t_f, i.e. the time it takes for the waveform to fall from 90% to 10% of its amplitude, which is a measure of the duration of the falling edge (also called the trailing edge).

Other nonidealities (e.g. overshoots, settling time, jitter) usually do not affect the macroscopic operation of model (academic, ideal) converters. We will therefore neglect them. However, taking them into account becomes necessary at the optimization stage of physical (real) circuits where they can cause undesirable microscopic phenomena adversely affecting the overall system operation.

3. Buck Converter

3.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
B	Eri	2.1, 2.2	2.3.a,b,d, 3.1.b, 3.2.a—b		
			3.1.c—f		3.2
E	Eri	4, 4.1.1, 4.1.5	3.1.c, 3.2.c		
F	Eri	4.3, 4.3.1	3.3.a,f; #3[A] 3.3.c		
			3.2.d, 3.3.b—f		3.3
			3.4		3.4

3.2. Buck converter passive components

3.2.a. Inductor effect

The role of the two passive components of the buck DC/DC converter—the inductor (choke) and capacitor—may be analysed from the signal point of view (low-pass filtering) but also from the power transmission point of view. Most receivers (e.g., microprocessors) require constant power supply. A buck converter without an LC filter is called 'voltage chopper' because its input voltage appears at the receiver as 'chopped'. Power flow is therefore temporarily and periodically interrupted.

Wired power transmission necessitates charge motion in a conductor, or current. Thus, constant power delivery necessitates uninterrupted current flow. To obtain it, a component should be inserted into the circuit that will prevent the output current from immediately dropping down to zero in the moment of switch opening. The inductor is well known for this property which follows from energy conservation principle. It says that any change in energy of a system (in this case, the inductor) may only result from additional energy being delivered from outside. No energy can be delivered in zero time as this would necessitate infinite instantaneous power

$$p = \frac{\mathrm{d}W}{\mathrm{d}t} \tag{3.1}$$

which is unrealistic. Thus, neither can inductor's energy change abruptly. This energy W_L is accumulated in magnetic field caused by the current i_L flowing through the inductor; they are related to each other by

$$W_\mathrm{L} = \frac{L i_\mathrm{L}^2}{2} \tag{3.2}$$

where L is the inductance of the inductor. Therefore, the current through an inductor cannot change abruptly.

In order to make current through the receiver (load) continuous, the inductor must be inserted so as the receiver current i_o flows through it, thus in series. This is shown in Fig. 2(a).

3.2.b. Analytical description of the inductor

In each of the two sub-intervals of the switching period, the inductor is found in a series RL circuit which is described with Kirchhoff's voltage law

$$E = v_\mathrm{L} + v \tag{3.3}$$

where v_L is the voltage across the inductor and E is an effective forced voltage which is V_g in sub-interval 1 (Fig. 3a) and 0 in sub-interval 2 (short-circuit which is equivalent to zero voltage source, Fig. 3b). Using Ohm's law and inductor equation and taking into account that $i_\mathrm{o} = i_\mathrm{L}$ during both subintervals, we obtain the equation of the RL circuit

$$R i_\mathrm{o} + L \frac{\mathrm{d}i_\mathrm{o}}{\mathrm{d}t} - E = 0 \tag{3.4}$$

Using any method of differential equation solution, the solution is found to be

$$i_\mathrm{o}(t) = i_\mathrm{o}(t_0) + \left(\frac{E}{R} - i_\mathrm{o}(t_0) \right) \cdot \left(1 - \mathrm{e}^{-\frac{t-t_0}{\tau}} \right) \tag{3.5}$$

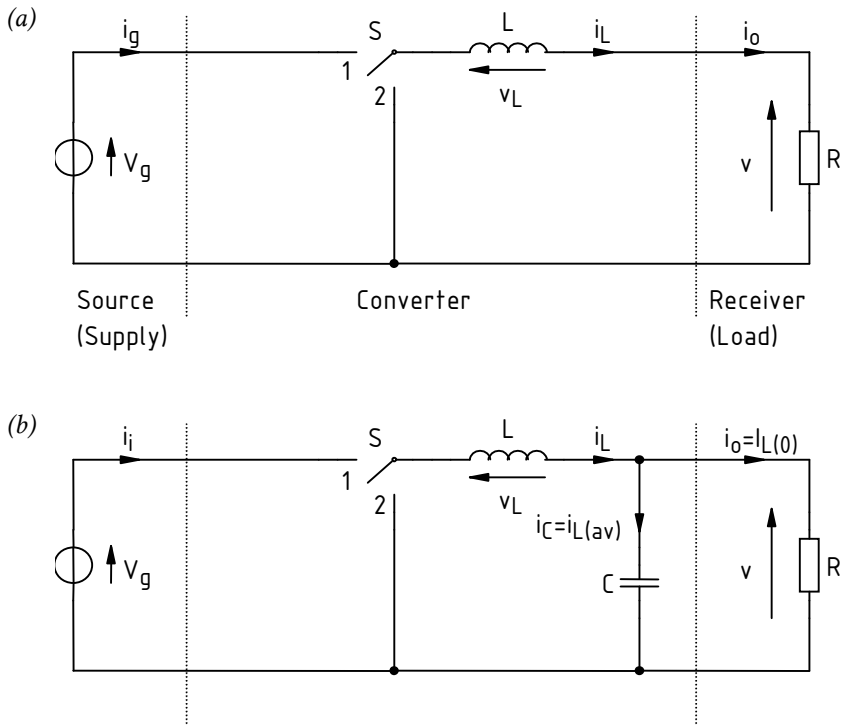

Fig. 2. Buck converter circuit: (a) with only the inductor; (b) with the capacitor added

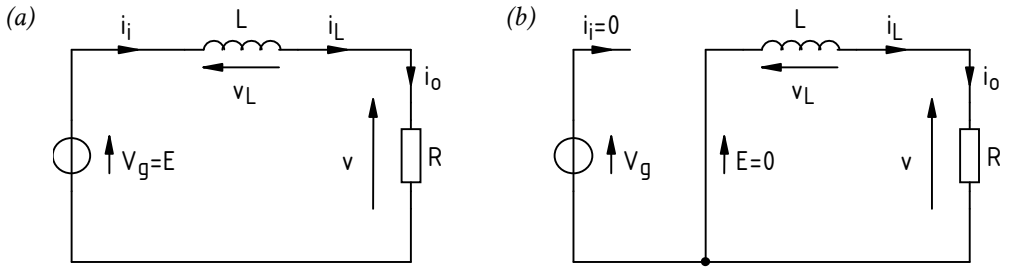

Fig. 3. Reduced circuit topology of Fig. 2(a): (a) during sub-interval 1; b) during sub-interval 2

where τ is called the time constant and equals

$$\tau = \frac{L}{R} \tag{3.6}$$

and t_0 denotes the beginning of a given sub-interval. Let us apply Eq. (3.5) to either sub-interval.

1. For sub-interval 1, $t_0 = t_1$. Assume that the current is zero initially: $i_o(t_0) = 0$. Then,

$$i_o(t) = \frac{V_g}{R} \cdot \left(1 - e^{-\frac{t-t_1}{\tau}}\right) \tag{3.7}$$

Substituting $t = t_1$ and $t = \infty$ we have

$$i_o(t_1) = \frac{V_g}{R} \cdot \left(1 - e^{-\frac{t_1-t_1}{\tau}}\right) = \frac{V_g}{R} \cdot \left(1 - e^{-0}\right) = \frac{V_g}{R} \cdot (1-1) = 0 \tag{3.8}$$

which complies with our assumption, and

$$i_{\mathrm{o}}(\infty)=\frac{V_{\mathrm{g}}}{R}\cdot\left(1-\mathrm{e}^{-\frac{\infty-t_1}{\tau}}\right)=\frac{V_{\mathrm{g}}}{R}\cdot\left(1-\mathrm{e}^{-\infty}\right)=\frac{V_{\mathrm{g}}}{R}\cdot\left(1-\frac{1}{\mathrm{e}^{\infty}}\right)=\frac{V_{\mathrm{g}}}{R}\cdot\left(1-\frac{1}{\infty}\right)=$$
$$=\frac{V_{\mathrm{g}}}{R}\cdot(1-0)=\frac{V_{\mathrm{g}}}{R} \tag{3.9}$$

The current therefore changes exponentially, rising from 0 up to V_{g}/R. This has been illustrated in Fig. 4(a).

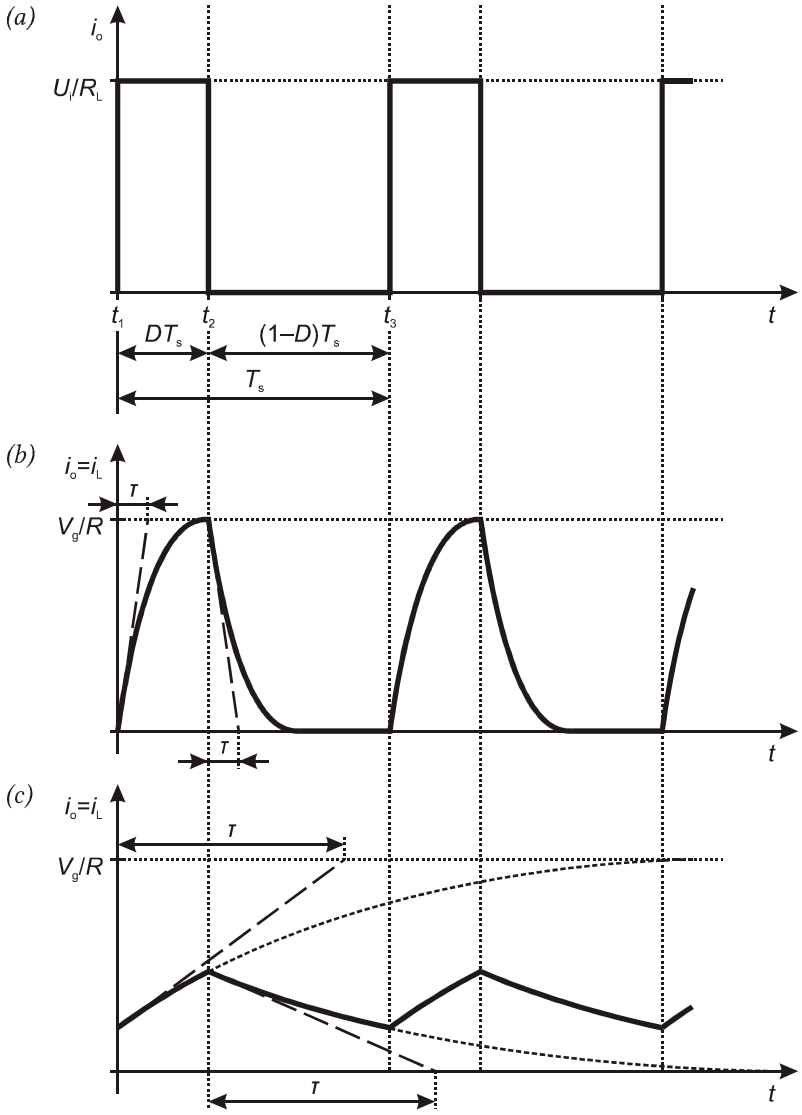

Fig. 4. Output current waveform: (a) without an inductor; (b) with an inductor (Fig. 2a) of small inductance ($\tau \ll T_{\mathrm{s}}$); (c) with an inductor if large inductance ($\tau \approx T_{\mathrm{s}}$)

2. At the beginning of sub-interval 2 ($t_0 = t_2$), the current equals that at the end of sub-interval 1. We therefore obtain

$$i_{\mathrm{o}}(t)=\frac{V_{\mathrm{g}}}{R}-\frac{V_{\mathrm{g}}}{R}\cdot\left(1-\mathrm{e}^{-\frac{t-t_2}{\tau}}\right)=\frac{V_{\mathrm{g}}}{R}\cdot\left(1-1+\mathrm{e}^{-\frac{t-t_2}{\tau}}\right)=\frac{V_{\mathrm{g}}}{R}\cdot\mathrm{e}^{-\frac{t-t_2}{\tau}} \tag{3.10}$$

Substituting $t = t_2$ and $t = \infty$ we have

$$i_o(t_2) = \frac{V_g}{R} \cdot e^{-\frac{t_2 - t_2}{\tau}} = \frac{V_g}{R} \cdot e^{-0} = \frac{V_g}{R} \cdot 1 = \frac{V_g}{R} \tag{3.11}$$

which complies with our assumption, and

$$i_o(\infty) = \frac{V_g}{R} \cdot e^{-\frac{\infty - t_2}{\tau}} = \frac{V_g}{R} \cdot e^{-\infty} = \frac{V_g}{R} \cdot 0 = 0 \tag{3.12}$$

The current therefore changes exponentially, falling from V_g/R down to 0. This has been illustrated in Fig. 4(b).

The time of current settling down depends on the time constant τ. It can be calculated that its steady-state value is reached with an accuracy of 1% (0,01) after a time equal $\tau \ln(1/0{,}01) \approx 4{,}6\tau$. It therefore follows from (3.6) that the larger the inductance (for given R), the slower the current rise and thus, the stronger the inductor opposes abrupt current changes. In power electronics, an inductor of an inductance large enough to visibly slow down current variation in time, is called a choke.

When choke inductance is sufficiently large, current is unable to attain the levels of V_g/R and 0 at the end of either sub-interval. This is demonstrated in Fig. 4(c). In general, a simplified condition for this occurring can be written down as

$$4\tau > T_s \tag{3.13}$$

where the number 4 results from rounding the value of 4,6 justified above. Substituting (3.6)

$$L > \frac{R}{4 f_s} \tag{3.14}$$

As inductor current also flows through the load resistance R, i_o current has the exact shape of i_L. According to Ohm's law, voltage v across the load resistance must also be of the same form.

3.2.c. Capacitor effect

Using the inductor, we gained continuous output voltage, but it is still far from being constant. In most applications, minimising voltage ripple using only an inductor is impossible as it would result in unacceptable size, weight, cost and power loss. Moreover, an inductor is not capable of filtering high-frequency disturbance (short spikes and fast oscillations) that are inherently linked with switched-mode power converters.

For the above reasons, a second type passive component must be used: a capacitor. Its energy is expressed as

$$W_C = \frac{C v_C^2}{2} \tag{3.15}$$

where C is the capacitor's capacitance and v_C is the voltage across it. It therefore follows from energy conservation principle that voltage across a capacitor cannot change abruptly.

In order to make use of this property, the capacitor must be inserted so that the receiver's voltage v appears across it. Only then it will slow down the variation of this voltage in time. This leads to the parallel connection shown in Fig. 2(b).

3.2.d. Analytical description of the capacitor

After insertion of the capacitor, the inductor current i_L splits into two branches: the capacitor's one and the receiver's one. According to Kirchhoff's current law (cf. Fig. 2b)

$$i_{\mathrm{L}} = i_{\mathrm{C}} + i_{\mathrm{o}} \tag{3.16}$$

The inductor current can be considered as the sum of a DC component $I_{\mathrm{L}(0)}$ and an AC one $i_{\mathrm{L(a)}}$:

$$i_{\mathrm{L}} = I_{\mathrm{L}(0)} + i_{\mathrm{L(a)}} \tag{3.17}$$

where, based on Fourier analysis, the DC component is equal to the average value $i_{\mathrm{L(av)}}$ (level *I* in Fig. 2.10 of Ref. B). Consequently

$$i_{\mathrm{L(a)}} = i_{\mathrm{L}} - I_{\mathrm{L}(0)} = i_{\mathrm{L}} - i_{\mathrm{L(av)}} \tag{3.18}$$

It is therefore the i_{L} waveform shifted down by its own average value. The $i_{\mathrm{L(a)}}$ waveform has therefore exactly the same shape but it is varying under and over the time axis (and not under and over the DC level *I*).

The magnitude of a capacitor's impedance is given by

$$\left|Z_{\mathrm{C}}\right| = \frac{1}{\omega C} = \frac{1}{2\pi f C} \tag{3.19}$$

For $f \longrightarrow 0$ we have $|Z_{\mathrm{C}}| \longrightarrow \infty$ which means that for the DC component, a capacitor presents a gap in the circuit. Thus, no DC component can ever flow through a capacitor. On the other hand, high frequency current components (such as the converter's switching frequency f_{s}) will easily pass through as for $f \longrightarrow \infty$ we have $|Z_{\mathrm{C}}| \longrightarrow 0$.

It follows from (3.19) that the higher the capacitance *C*, the lower the impedance for a given frequency *f* will be. The capacitor C and the load resistance R form a current divider, whose action for a given frequency is described by the formulae

$$\begin{aligned} I_{\mathrm{C}(f)} &= I_{\mathrm{L}(f)} \frac{R}{\left|Z_{\mathrm{C}}(f)\right| + R} = I_{\mathrm{L}(f)} \frac{1}{1 + \dfrac{\left|Z_{\mathrm{C}}(f)\right|}{R}} \\ I_{\mathrm{o}(f)} &= I_{\mathrm{L}(f)} \frac{\left|Z_{\mathrm{C}}(f)\right|}{\left|Z_{\mathrm{C}}(f)\right| + R} = I_{\mathrm{L}(f)} \frac{1}{1 + \dfrac{R}{\left|Z_{\mathrm{C}}(f)\right|}} \end{aligned} \tag{3.20}$$

where $I_{(f)}$ is the rms value of a sine wave current of frequency *f*. The above relationships can be interpreted as follows:

- the lower the capacitor's impedance for a given frequency *f* as related to the load resistance, the greater part of a current of this frequency $I_{\mathrm{C}(f)}$ will flow through the capacitor (the denominator in $I_{\mathrm{C}(f)}$ formula decreases, so the whole expression increases);
- thus, the smaller part $I_{\mathrm{o}(f)}$ will flow through the receiver (the denominator in $I_{\mathrm{o}(f)}$ formula increases, so the whole expression decreases).

In the circuit under consideration, we want to eliminate the AC component from the i_{o} waveform. Then, the output current i_{o} will be constant and so will be the output voltage *v* across the load resistance (by Ohm's law). As we have noted, the DC component of the inductor current cannot flow through the capacitor, thus it entirely flows to the receiver:

$$\begin{aligned} I_{\mathrm{C}(0)} &= 0 \\ I_{\mathrm{o}(0)} &= I_{\mathrm{L}(0)} \end{aligned} \tag{3.21}$$

We could obtain the same result by substituting (3.19) and $f = 0$ into (3.20). How to redirect the AC component to the capacitor? It follows from (3.20) that the condition is

$$\left|Z_{\mathrm{C}}(f)\right| << R_{\mathrm{L}} \Leftrightarrow \frac{\left|Z_{\mathrm{C}}(f)\right|}{R_{\mathrm{L}}} << 1 \tag{3.22}$$

because then

$$I_{\mathrm{C}(f)} = I_{\mathrm{L}(f)} \frac{1}{1+\dfrac{\left|Z_{\mathrm{C}}(f)\right|}{R_{\mathrm{L}}}} \approx I_{\mathrm{L}(f)} \frac{1}{1} = I_{\mathrm{L}(f)} \tag{3.23}$$

However, capacitor impedance Z_{C} is dependent on frequency. As we have stated above, the inductor current AC component $i_{\mathrm{L(a)}}$ is of triangular shape. Based on Fourier analysis, it can be represented by a sum of sine waveforms whose frequencies are f_{s} and its odd multiples. Therefore, if the condition (3.22) is fulfilled for the frequency of f_{s}, it is also fulfilled for the entire AC component of inductor current. This is because other sine waveforms are of greater frequencies ($3f_{\mathrm{s}}$, $5f_{\mathrm{s}}$ etc.) and $|Z_{\mathrm{C}}|$ decreases with frequency. Thus, the entire AC component of inductor current will flow through the capacitor. By substituting (3.19), we obtain the condition (3.22) in the form of

$$C >> \frac{1}{2\pi f_{\mathrm{s}} R_{\mathrm{L}}} \tag{3.24}$$

3.3. Effect of transistor power loss on converter characteristics

3.3.a. Input current

To conduct an energetic analysis of the converter, in order to determine the input power we will need to know the DC component of the input current i_i. As we have already noticed in Section 3.3.a, it is equal to the inductor current i_L during sub-interval 1 and zero during sub-interval 2 (see Fig. 3, and Fig. 2.8 in Ref. B); hence, by definition of the average value,

$$I_{\mathrm{i}(0)} = i_{\mathrm{i(av)}} = \frac{1}{T_\mathrm{s}} \int_{DT_\mathrm{s}} i_\mathrm{i}\,\mathrm{d}t = \frac{1}{T_\mathrm{s}} \left(\int_{DT_\mathrm{s}} i_\mathrm{L}\,\mathrm{d}t + \int_{(1-D)T_\mathrm{s}} 0\,\mathrm{d}t \right) = \frac{1}{T_\mathrm{s}} \int_{DT_\mathrm{s}} i_\mathrm{L}\,\mathrm{d}t \tag{3.25}$$

Let us mathematically transform the result obtained:

$$I_{\mathrm{i}(0)} = D \times \frac{1}{DT_\mathrm{s}} \int_{DT_\mathrm{s}} i_\mathrm{L}\,\mathrm{d}t \tag{3.26}$$

The expression after the multiplication sign is by definition the average value of the inductor current i_L over the time interval DT_s, i.e. the transistor's on state duration. This current's waveform is triangular (see Fig. 2.10 in Ref. B), so it consists of two sections of linear rise or fall. It is easy to show (either by simple reasoning or formally by integration) that the average value of such a waveform is simply equal to the average of the peak and valley values, and that it applies equally to the entire period and for each interval separately. Thus, the average over the DT_s sub-interval can be replaced by the average value over the entire period $i_{\mathrm{L(av)}}$, or the DC component $I_{\mathrm{L}(0)}$:

$$I_{\mathrm{i}(0)} = D i_{\mathrm{L(av)}} = D I_{\mathrm{L}(0)} \tag{3.27}$$

Using (3.21), we finally obtain:

$$I_{\mathrm{i}(0)} = D I_\mathrm{o} = D \frac{V}{R} \tag{3.28}$$

Thus, in the buck converter, the input current is less than the output current (load) by the same ratio as the output voltage is less than the input voltage [see Eq. (2.24) in Ref. B].Taking into account (2.24) from Ref. B, the above equation may be converted to a form dependent on the input voltage:

$$I_{\mathrm{i}(0)} = D^2 \frac{V_\mathrm{g}}{R} \tag{3.29}$$

The resulting theoretical expression will be useful when carrying out the exercise for checking if the system is not drawing too much current, which would indicate an error or malfunction. Then, the knowledge of the theoretical input current will be needed also for the circuit from which the discussion was started, i.e. the one without passive components (Ref. B of Manual 0). In this case, the input current i_i equals the output current I_o during sub-interval 1 and zero in sub-interval 2 (cf. Fig. 1.8 in Ref. B of Manual 0).Thus, its DC component is

$$I_{\mathrm{i}(0)} = i_{\mathrm{i(av)}} = \frac{1}{T_\mathrm{s}} \int_{DT_\mathrm{s}} i_\mathrm{i}\,\mathrm{d}t = \frac{1}{T_\mathrm{s}} \cdot \left(\int_{DT_\mathrm{s}} i_\mathrm{o}\,\mathrm{d}t + \int_{(1-D)T_\mathrm{s}} 0\,\mathrm{d}t \right) = \frac{1}{T_\mathrm{s}} \cdot \left(\int_{DT_\mathrm{s}} \frac{V_\mathrm{g}}{R}\,\mathrm{d}t + 0 \right) = \frac{1}{T_\mathrm{s}} \cdot \frac{V_\mathrm{g}}{R} DT_\mathrm{s} = D \frac{V_\mathrm{g}}{R} \tag{3.30}$$

A comparison of this result with (3.29) leads to the observation that for $D < 1$, the DC component of the input current is higher when there is no filter in the circuit. It can be easily demonstrated that this results from the fact that the active output power in either case is also different, despite the same average value of the output voltage. Depending on the waveform—pulse

wave without a filter, constant with a filter—this voltage has different rms values which is what active power depends on.

3.3.b. Effect of static power loss on efficiency

It would be a complicated task to derive an analytical expression for converter efficiency. However, we can easily state what influence on the efficiency has the MOSFET transistor investigated in this exercise. To limit the number of necessary assumptions for this device parameter values, we will begin with static power loss only. We will also assume that inductor current ripple is negligible as compared to its DC component; the inductor current may therefore be considered as constant, equal $I_{\mathrm{L(0)}}$.

The converter's average input power is

$$P_{\mathrm{i}} = \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} u_{\mathrm{i}} i_{\mathrm{i}} \mathrm{d}t = V_{\mathrm{g}} \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} i_{\mathrm{i}} \mathrm{d}t = V_{\mathrm{g}} i_{\mathrm{i(av)}} = V_{\mathrm{g}} I_{\mathrm{i(0)}} \tag{3.31}$$

so it is the product of the constant input voltage and the DC component of the input current. The latter is expressed with equation (3.27), hence finally

$$P_{\mathrm{i}} = D V_{\mathrm{g}} I_{\mathrm{L(0)}} \tag{3.32}$$

Static power loss in the transistor is $I_{\mathrm{L(0)}}{}^2 R_{\mathrm{DS(on)}}$ (see Manual 3$^{\mathrm{A}}$, Ref. A) during sub-interval 1 and virtually zero during sub-interval 2 (off state). Therefore, average static power loss is

$$P_{\mathrm{T,stat}} = \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} p_{\mathrm{Ts}} \mathrm{d}t = \frac{1}{T_{\mathrm{s}}} \cdot \left(\int_{DT_{\mathrm{s}}} I_{\mathrm{L(0)}}^2 R_{\mathrm{DS(on)}} \mathrm{d}t + \int_{(1-D)T_{\mathrm{s}}} 0 \, \mathrm{d}t \right) = \frac{1}{T_{\mathrm{s}}} \cdot I_{\mathrm{L(0)}}^2 R_{\mathrm{DS(on)}} D T_{\mathrm{s}} = D I_{\mathrm{L(0)}}^2 R_{\mathrm{DS(on)}} \tag{3.33}$$

Assuming that the decrease in transmitted power which occurs between converter's input and output results only from the above static power loss in the transistor, we have

$$\eta = \frac{P_{\mathrm{o}}}{P_{\mathrm{i}}} = \frac{P_{\mathrm{i}} - P_{\mathrm{T,stat}}}{P_{\mathrm{i}}} = 1 - \frac{P_{\mathrm{T,stat}}}{P_{\mathrm{i}}} = 1 - \frac{I_{\mathrm{L(0)}}}{V_{\mathrm{g}}} R_{\mathrm{DS(on)}} \tag{3.34}$$

Applying Ohm's law to the receiver, we obtain

$$\eta = 1 - \frac{V}{V_{\mathrm{g}}} \frac{R_{\mathrm{DS(on)}}}{R} \tag{3.35}$$

3.3.c. Effect of static power loss on voltage conversion ratio

To obtain a more informative form of (3.35), we must derive a relationship between input and output voltage. We cannot use the relationship from Ref. B because it has been derived for the ideal switch. Taking into account the non-zero on-state voltage drop across the transistor $V_{\mathrm{DS(on)}}$ (see Manual 3$^{\mathrm{A}}$, Ref. A), the voltage across the inductor for sub-interval 1 must be expressed as

$$\begin{aligned} v_{\mathrm{L}} &= V_{\mathrm{g}} - V - v_{\mathrm{T}} = V_{\mathrm{g}} - V - V_{\mathrm{DS(on)}} = V_{\mathrm{g}} - V - I_{\mathrm{L(0)}} R_{\mathrm{DS(on)}} = \\ &= V_{\mathrm{g}} - V - \frac{V}{R} R_{\mathrm{DS(on)}} = V_{\mathrm{g}} - V \left(1 + \frac{R_{\mathrm{DS(on)}}}{R} \right) \end{aligned} \tag{3.36}$$

The change of inductor current during sub-interval 1 is therefore (cf. Ref. B and Fig. 3)

$$(2\Delta i)_1 = \frac{\left[V_\mathrm{g} - V\left(1 + \dfrac{R_{\mathrm{DS(on)}}}{R}\right)\right] \cdot DT_\mathrm{s}}{L} \tag{3.37}$$

while during sub-interval 2 it is

$$(2\Delta i)_2 = \frac{-V \cdot (1-D)T_\mathrm{s}}{L} \tag{3.38}$$

By equating the above expressions and rearranging, we get

$$V = V_\mathrm{g} \frac{D}{1 + D\dfrac{R_{\mathrm{DS(on)}}}{R}} \tag{3.39}$$

Hence, the voltage conversion ratio [denoted $M(D)$ in Ref. B], defined as

$$K_U \equiv M(D) = \frac{U_\mathrm{o}}{U_\mathrm{i}} \tag{3.40}$$

where U_o and U_i are output and input voltages, respectively, is

$$K_U = \frac{V}{V_\mathrm{g}} = \frac{D}{1 + D\dfrac{R_{\mathrm{DS(on)}}}{R_\mathrm{L}}} \tag{3.41}$$

For $R_{\mathrm{DS(on)}} = 0$, these reduce to the ideal converter formulae [see Ref. B, equation (2.24) and Fig. 2.5(a)]. In a real converter, the output voltage decreases with an increasing ratio of transistor's on-state resistance to load resistance. The discrepancy between ideal and real converter also increases when the duty cycle D is increased.

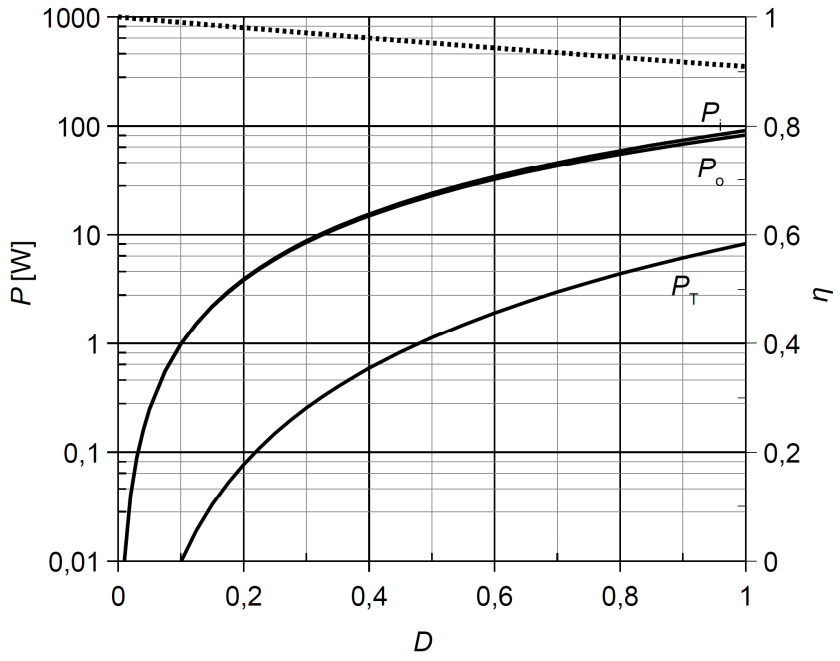

Fig. 5. Average power (solid lines) and converter efficiency η (dotted line) as a function of duty cycle D (only static power loss in the transistor is considered), for the circuit parameters: V_g = 10 V, R = 1 Ω, $R_{DS(on)}$ = 0.1 Ω

3.3.d. Converter characteristics considering transistor static power loss

By substituting (3.39) to (3.35), we obtain

$$\eta = 1 - \frac{D}{1 + D\dfrac{R_{\mathrm{DS(on)}}}{R}} \frac{R_{\mathrm{DS(on)}}}{R} = 1 - \frac{1}{1 + \dfrac{1}{D}\dfrac{R}{R_{\mathrm{DS(on)}}}} = \frac{1}{1 + D\dfrac{R_{\mathrm{DS(on)}}}{R}} \tag{3.42}$$

This relationship has been plotted in Fig. 5 for an exemplary ratio of $R_{\mathrm{DS(on)}}/R = 0.1$ which is quite a large value, chosen to highlight the observed decrease in efficiency. In fact, a transistor with a resistance 10 times lower than the load resistance would be considered improperly selected for a given application. Nevertheless, even under such a high resistance ratio, the efficiency only drops to approx. 0.9 for $D = 1$.

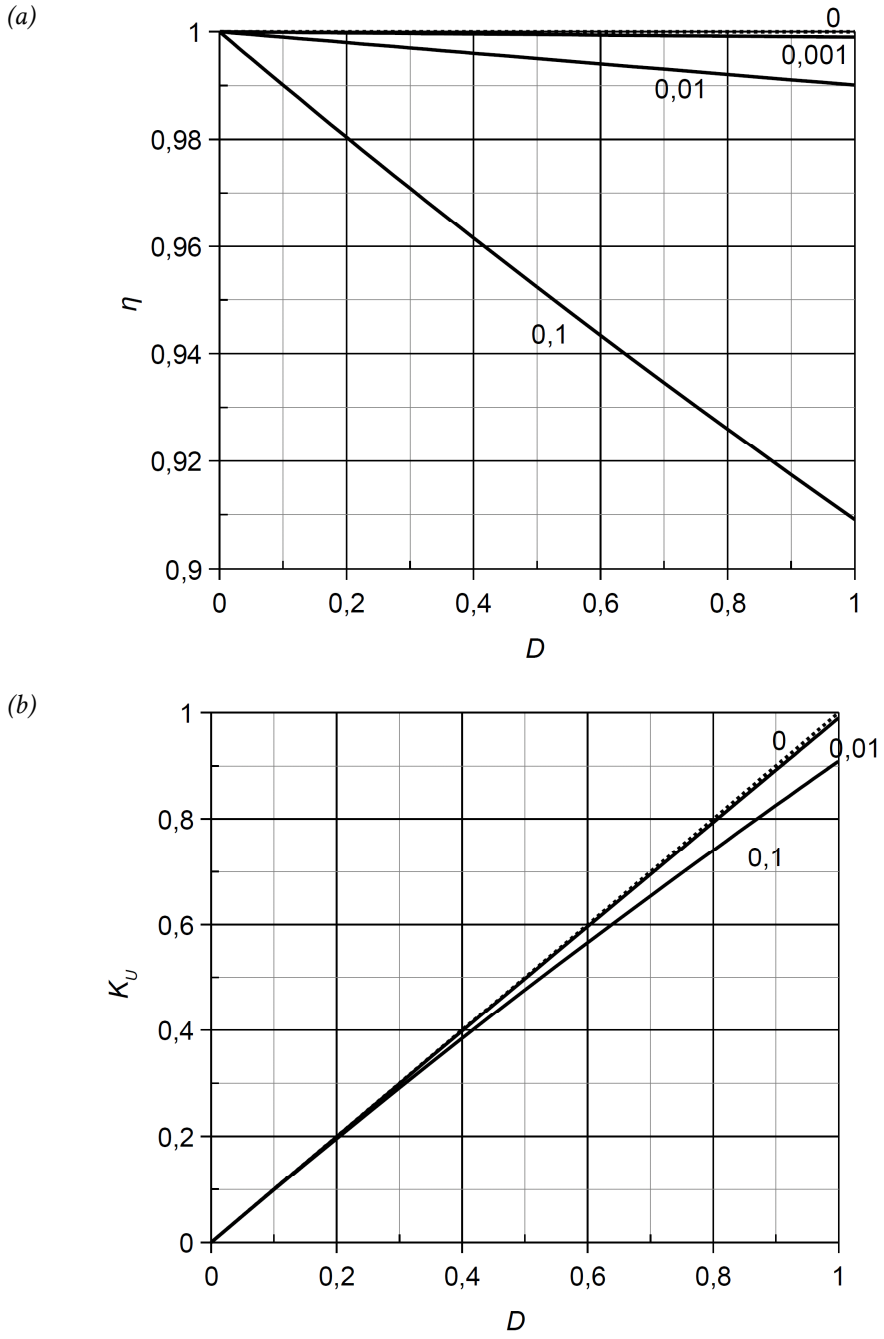

Fig. 6. Converter characteristics as a function of duty cycle D and $R_{\mathrm{DS(on)}}/R$ ratio (only transistor static power loss has been considered; the value of 0 and the dotted line correspond to the ideal converter): (a) efficiency; (b) voltage conversion ratio

Thus, the buck converter is not particularly demanding in terms of transistor parameters. Even with a poorly selected transistor we get an energy conversion efficiency much higher than in the case of linear mode circuits (Manual 0, Ref. E). The buck converter has therefore a high efficiency in the entire range of the duty cycle. This makes the step-down topology stand up among DC converters.

As follows from (3.42), for $R_{DS(on)} \longrightarrow 0$ and for $D \longrightarrow 0$, the efficiency tends to unity. On the other hand, when the duty cycle is increased, efficiency decreases. This decrease is stronger for a higher transistor to load resistance ratio. This is confirmed by Fig. 6(a) where efficiency characteristics have been plotted for various $R_{DS(on)}/R$ ratios.

Fig. 6(b) shows the voltage conversion ratio characteristic (3.41). It also proves that in the case of the buck converter, an apparent deviation from the ideal characteristic is only observed when the transistor is exceptionally poorly selected.

3.3.e. Effect of dynamic power loss

To simplify the problem, let us assume that turn-on and turn-off times are equal to a common value of t_{sw}. Then, transistor dynamic power loss is (see Ref. F)

$$P_{T,dyn} = (\tfrac{1}{2} I_{L(0)} V_g t_{sw} + \tfrac{1}{2} I_{L(0)} V_g t_{sw}) f_s = I_{L(0)} V_g t_{sw} f_s \tag{3.43}$$

Using (3.32) and assuming that transistor dynamic power loss is the only cause for efficiency decrease, we obtain the formula

$$\eta = \frac{P_o}{P_i} = \frac{P_i - P_{T,dyn}}{P_i} = 1 - \frac{P_{T,dyn}}{P_i} = 1 - \frac{t_{sw} f_s}{D} = 1 - \frac{1}{D}\frac{t_{sw}}{T_s} \tag{3.44}$$

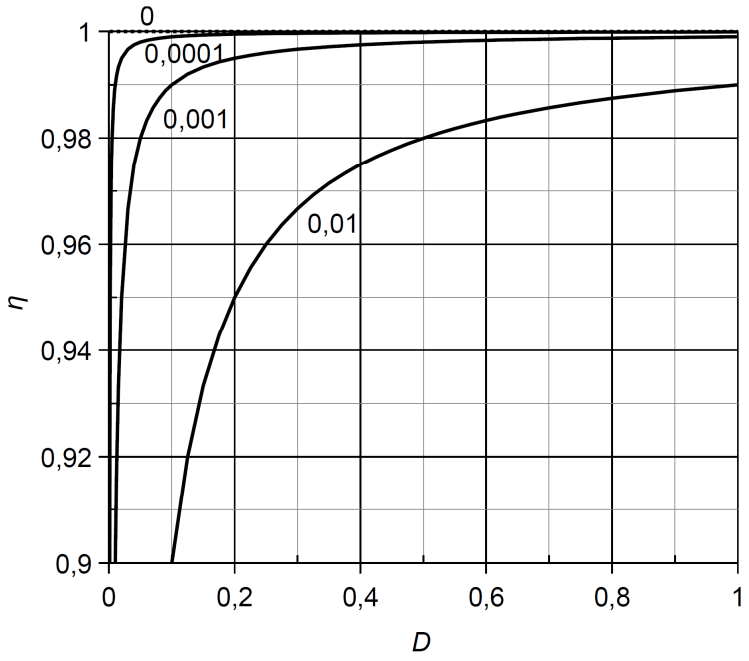

Fig. 7. Characteristics of efficiency vs. duty cycle D and t_{sw}/T_s ratio (only transistor dynamic power loss has been considered; the value of 0 and the dotted line correspond to the ideal converter)

The above relationship has been plotted in Fig. 7 for different transistor switching time t_{sw} to converter switching period T_s ratios. It can be seen that the effect of transistor dynamic power loss is different than that of static loss: efficiency decreases with decreasing duty cycle. The higher the

t_{sw}/T_s ratio, the more important this decrease is; for example, a ratio of 0.001 corresponds to t_{sw} = 100 ns at f_s = 10 kHz, or t_{sw} = 10 ns at f_s = 100 kHz.

3.3.f. Switching frequency and MOSFET application

It should be remembered that our aim has been to assess the effect of transistor power loss only. In a real circuit, power losses are also present in the diode and the passive components (inductor and capacitor). They cause a further decrease in efficiency and voltage conversion ratio, for both high and low duty cycle values.

The effectiveness of both the inductor and the capacitor is tightly linked to their values. As shown in Ref. B and Section 3, assuring a constant current flow requires an adequately large inductance, and eliminating the output voltage ripple needs a large enough capacitance. It therefore follows from (3.2) and (3.15) that these elements must have an adequate energy storage capability which in turn requires important dimensions. At the same time, passive element stay resistance will be large which will result in an increase in converter power loss and a decrease in its efficiency.

However, let us take a look at Fig. 4 which—as far as waveform shapes are concerned—applies to both the inductor with its current and to the capacitor with its voltage. From this set of plots, it can be deduced that if the duration of both sub-intervals is decreased proportionally—which is equivalent to increasing the switching frequency f_s—the current will rise and fall by a smaller amount. The ripple will therefore be minimised and so the passive element will become more effective. The output voltage will not be affected because—as shown in ref. B—it is not dependent on the switching period T_s but on the duty cycle D which is the mutual ratio of sub-intervals' durations. An inverse reasoning leads to the conclusion that a same effectiveness can be obtained using an inductor with smaller inductance. The same applies to the capacitor's capacitance.

The above conclusion is the main reason for a high operating frequency of any switched-mode power converter. However, the relationships derived in Ref. F and in Section 3.3.f reveals that this causes the dynamic power loss in the transistor to increase. This can only be compensated by using a semiconductor switch with high switching speed, i.e., shorted switching times, the decrease in efficiency being dependent on the $t_{sw}f_s$ product (cf. Fig. 7). At present, MOSFETs are the controlled power semiconductor devices with the shortest switching times. This explains their dominance in switched-mode DC/DC power converters.

Additional profits from MOSFET application comes from the field-effect control mechanism that results in:

1° very low a drive power (both with respect to the power processed in the system and to the power loss in the transistor's main circuit) which does not lower the system efficiency as it is in the case of the current-driven BJTs;

2° the possibility to drive the transistor directly from the outputs of integrated circuits (as driving signal is essentially a voltage and not a current), which simplifies the realisation of digital control systems.

3.4. Power-based approach to converter analysis

3.4.a. Relation of voltage conversion ratio to efficiency

A simple comparison of Figs. 6(a) and 6(b) leads to the significant observation that the deviation from the ideal conversion characteristic is the more apparent, the more efficiency deviates from its ideal value ($\eta = 1$).Intuitively, this can be explained as follows. Producing a specific output voltage V requires a current of V/R to flow through the receiver and therefore to deliver to the output a specific power equal

$$P_{\mathrm{o}} = VI_{\mathrm{o}} = \frac{V^2}{R} \tag{3.45}$$

At an efficiency of $\eta < 1$, a portion of the input power is lost in the converter and therefore does not reach the receiver. If so, then the output power is less; hence, by reversing the above formula to the form

$$V = \sqrt{P_{\mathrm{o}} R} \tag{3.46}$$

we come to the conclusion that the output voltage will be less than expected.

To express the above relation quantitatively, one must refer to the energy equation of the converter, i.e. to the relationship between the active input and output power. It follows directly from the definition of efficiency:

$$P_{\mathrm{i}} = \frac{P_{\mathrm{o}}}{\eta} \tag{3.47}$$

Assuming a constant input voltage, the active input power P_{i} is given by equation (3.31), while the output power is expressed with equation (3.45).The above equation can therefore expanded to

$$V_{\mathrm{g}} I_{\mathrm{i(0)}} = P_{\mathrm{i}} = \frac{P_{\mathrm{o}}}{\eta} = \frac{VI_{\mathrm{o}}}{\eta} \tag{3.48}$$

As we stated in Section 3.3.a, the input current is equal to the inductor current for the time the transistor is on, which is what we derived (3.27) from. That relationship is also valid for a lossy converter, as it was derived from Kirchhoff's current law applied to the node in which the semiconductor switch connects to the choke; it must be always maintained, regardless of energy loss in the system. In turn, from Kirchhoff's current law for the output node and from the assumption of ideal filtration, we obtained (3.21). Both currents (the input and the output ones) can therefore be expressed through the DC component of the inductor current:

$$V_{\mathrm{g}} D I_{\mathrm{L(0)}} = \frac{VI_{\mathrm{L(0)}}}{\eta} \tag{3.49}$$

Hence, after transformation

$$K_U = \frac{V}{V_{\mathrm{g}}} = \eta D \tag{3.50}$$

By comparing the above result to the voltage conversion ratio for the ideal (lossless) converter (see Ref. B)

$$K_{U(\mathrm{id})} = D \tag{3.51}$$

we find that the voltage conversion ratio for the real (lossy) buck converter is lower by a ratio equal to this converter's efficiency:

$$K_U = \eta K_{U(\mathrm{id})} \tag{3.52}$$

In other words, if we apply a some specific voltage V_g at the converter's input and will control its transistor using a signal with a specific duty cycle D, then in a real buck converter we will obtain an output voltage less than in an ideal converter, by a ratio equal to the efficiency of the former.

Note that the result obtained is consistent with the relationships demonstrating the impact of static power loss in the transistor on circuit operation, derived in Section 3.3. This is because voltage conversion ratio (3.41) and efficiency (3.42) are in fact related to each other through (3.50).

3.4.b. The impact of power loss on the current input

Finally, let us return to the discussion started in Section 3.3.a. The result obtained there [equation (3.29)] can also be reached by means of energetic analysis, which is even simpler because by transforming (3.48), we directly get

$$I_{\mathrm{i}(0)} = \frac{P_\mathrm{o}}{\eta V_\mathrm{g}} = \frac{V}{V_\mathrm{g}} \frac{I_\mathrm{o}}{\eta} = I_\mathrm{o} \frac{K_U}{\eta} \tag{3.53}$$

The obtained relationship is in fact a generalisation of equation (3.27), which can be seen when (3.50) is substituted into the latter. That equation is valid only for a specific topology: the buck converter. In contrast, the energy equation (3.48) and the relationship (3.53) are universal: true not only for the real (lossy) buck converter but also in general for any DC converter. This is because the relationships used to derive them were not linked to any specific circuit topology, nor were they founded on the assumption of unit efficiency.

Formula (3.53) allows the designer to predict the input current necessary to convert the voltage at a given ratio K_U, at a given load I_o and an assumed efficiency η. It tells that the DC component of the input current is:

1° proportional to the output current by a ratio inverse to the ratio of voltages ($I_{\mathrm{i}(0)} / I_\mathrm{o} \propto V / V_\mathrm{g}$),

2° inversely proportional to the converter efficiency (which is a number less than 1 so dividing by it means increasing the result).

Thus, the converter will draw a greater input current (meaning the DC component) for:

1° a higher output to input voltage ratio, which means that when a converter steps down the voltage, then the input current is less than the output current, and vice versa,

2° a less efficient inverter, which follows directly from the energy equation (3.48) because for a given input voltage V_g, if efficiency η is lower, then delivering a given output power P_o requires a greater input current to flow in order for the left-hand and the right-hand sides of the equation to match.

C

Experiment

4. Measurements

4.1. The measurement set-up

A general schematic of the non-isolated buck DC/DC converter under investigation is shown in Fig. 8. Banana sockets at both extremities enable connecting a power supply (input voltage U_i) and a receiver (load) R_L. Permanently mounted in the circuit are: a semiconductor switch, i.e., the transistor T and the diode D, and the input capacitor C_i, whose task is to ensure a constant input voltage. A blue 2-pin screw terminal block enables mounting the choke (inductor) L or making a short-circuit. The capacitor C is mounted in additional banana connectors transversely plugged into the receiver's connectors.

Circuit component values are:

- load resistance R_L = 4,7 Ω,
- choke inductance L = 150 μH,
- output capacitor capacitance C = 100 μF.

Voltage potentials at the most important nodes of the circuit are accessible through banana sockets. Voltage measurements with oscilloscope probes are done using banana connectors with leads that enable attaching a probe. These connectors may be freely moved depending on current measurement needs. Current waveform observation is possible with clamping a current probe on one of the wires led out above the front panel (i_L, i_T, i_D) or on a wire directly connected to the circuit's input or output (i_i, i_o).

The pulse waveform u_g driving the transistor comes from an external function generator (u_{gen}). As the ground of the generator is earth-connected, grounds of all voltage probes (which are also earth-connected) would have to be connected to the same point. This would considerably hinder measuring voltages with respect to other nodes; therefore, an insulating semiconductor integrated circuit (an optocoupler) has been used, containing a light-emitting diode, a photodiode and a suitable conditioning circuit.

The signal u_{gen} coming from the generator passes through the optocoupler and is applied as u_g to the input of the gate driver. The driver outputs a waveform of identical shape but optimised for fast

power MOSFET switching: with a higher top level and steeper edges, also ensuring a sufficiently high instantaneous current.

The drive voltage u_g after passing through the optocoupler is accessible in a banana socket. However, it is only applied at the transistor's gate after a button on the front panel (omitted in Fig. 8) is pushed: a green one (to switch on for the time the button is kept pushed), or a red one (to switch on permanently). A yellow light indicates that the driver is activated.

The control (drive) circuit, i.e., the optocoupler's output and the gate driver, require a separate power supply U_{GG}. To energise the circuit, two power supplies will be used:

- a high current capability one, for the power loop (U_i),
- a standard one, for the control circuit (U_{GG}).

Depending on laboratory stand, oscilloscope images are recorded using WaveStar for Oscilloscopes (for the TDS224 oscilloscope) or OpenChoice Desktop (TDS1002B oscilloscope) applications. An appropriate procedure is described further in this manual with oscilloscope type designation given in cases where procedures differ.

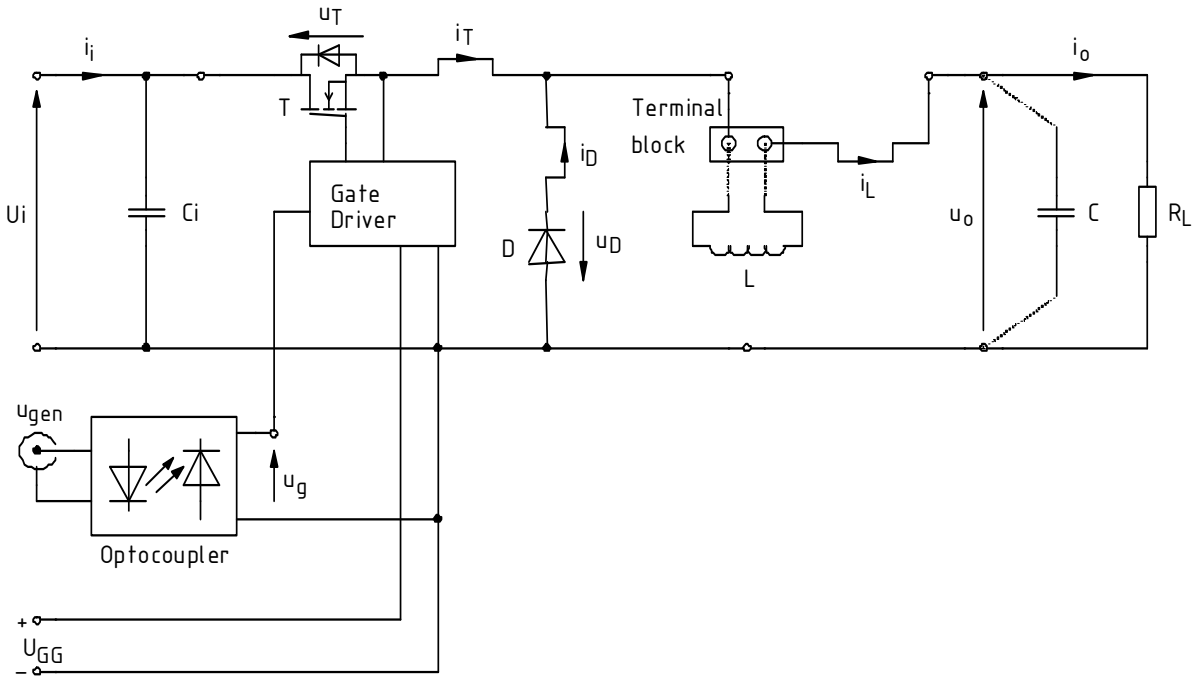

Fig. 8. Schematic of the buck DC/DC converter experimental set-up

4.2. Preparation for measurements

Configuring the measurement set-up

A block diagram of the measurement set-up is presented in Fig. 9 for two laboratory stands where this exercise can be carried out. It should be assembled and configured in the way described below and following the specified order of actions. If a specific oscilloscope model appears in a given step, it means that this step applies to this particular model, while it should not be carried out when another model is used.

To save time, you should proceed with subsequent steps in parallel with step 1.

1. Turn on your computer. After logon is completed, turn on the oscilloscope and set up its connection to the computer proceeding strictly according to the short manual available at the laboratory stand.
2. Ensure that power supplies are off. Connect:
   - a power supply with minimum current capability of 10 A and a minimum voltage capability of 40 V (which parameters are given on its housing), to the U_i input on the circuit's panel,
   - one of the adjustable sections of a standard 2- or 3-section power supply, to the control circuit supply input (U_{GG}).

   Do not safety-ground power supply using GND terminals.
3. Set the control circuit power supply into *Independent* mode using two buttons in the middle of its front panel.
4. Turn all the knobs of both power supplies to zero (extreme counterclockwise position).
5. Connect the receiver R_L, which is a set of resistors mounted on a heat sink, to the output (u_o) of the circuit under investigation.
6. Using a bare shorting wire available at the laboratory stand, short the two terminals of the blue screw terminal block.
7. Using a T-joint, connect the output of the function generator (*Main Output*) to both:
   - the u_{gen} input of the circuit under investigation and
   - [TDS224] the channel 3 input of the oscilloscope,
   - [TDS1002B] the external triggering (*Ext Trig*) input of the oscilloscope.
8. Connect voltage probes with 1:10 attenuation ([TDS1002B] which is selected with a switch on the probe body, 10x) attached to oscilloscope inputs so as to measure:
   (a) the transistor's gate drive voltage u_g on channel 1;
   (b) [TDS224] the converter's output voltage u_o on channel 2.

   The grounds of the voltage probes are connected to each other and connected to the mains protective ground inside the oscilloscope; therefore they must be connected to the same potential. Other connection may result in current flow through the oscilloscope and damage of its input circuitry!
9. Generate the driving waveform:
   (a) turn on the function generator;
   (b) from the web page, obtain and write down the converter switching frequency f_s;

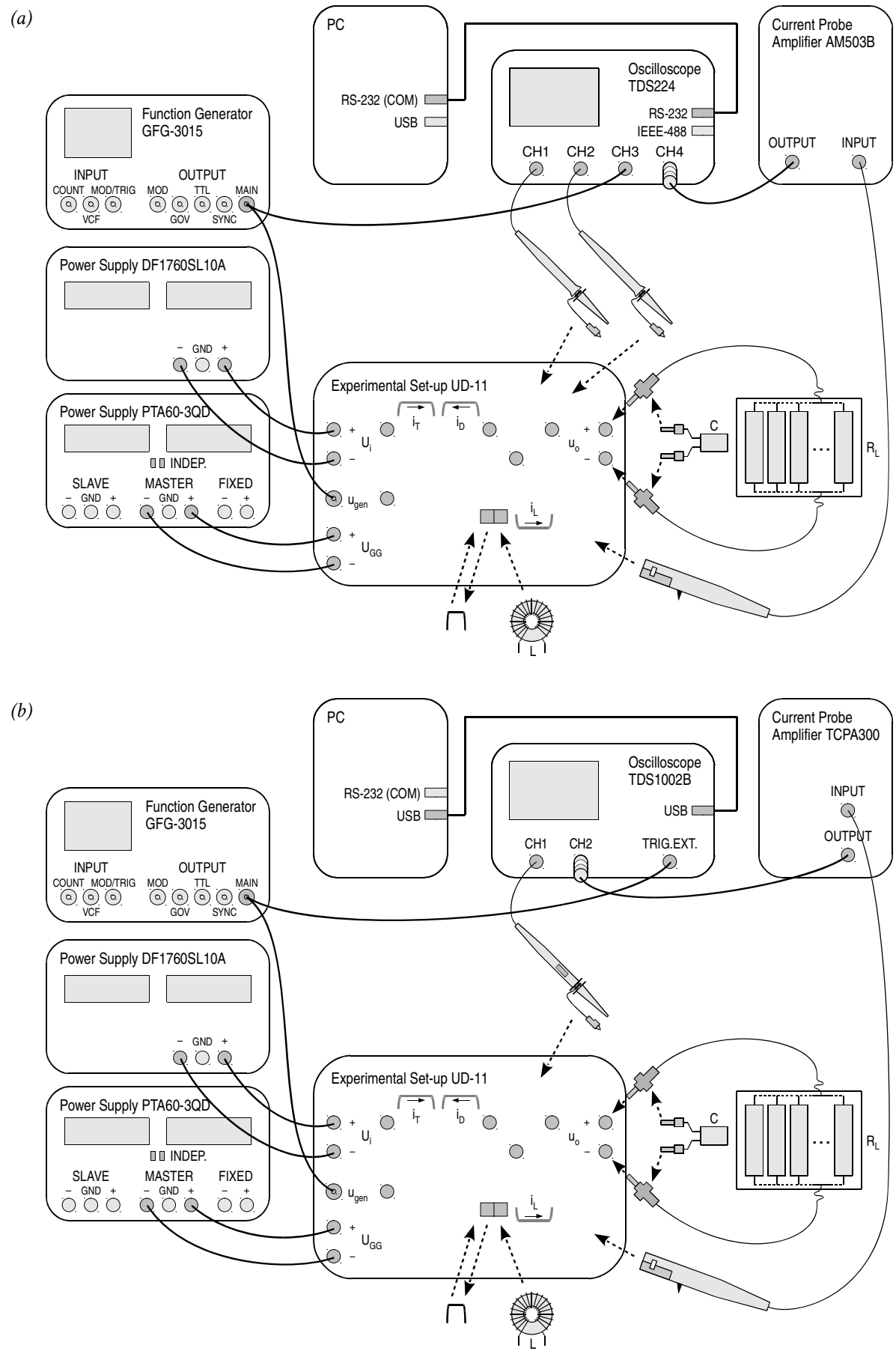

Fig. 9. Block diagram of the measurement set-up for time waveforms recording: (a) with the TDS224 oscilloscope; (b) with the TDS1002B oscilloscope

(c) on the generator:

A value entered with the keyboard is confirmed by pushing an appropriate unit button to the right.

- choose rectangular wave (*Func* button),
- set amplitude (*Ampl*) to 10 V (peak-to-peak value, *Vpp*),
- set frequency (*Freq*) to the one determined above,
- set duty cycle (*Duty*) to $D = 0.35$ (the duty cycle is expressed as percentage on the generator).

Before proceeding, connections in the circuit must be checked by the teacher!

While performing the next step, pay special attention to not exceeding at any time the value of 18 V. Otherwise, integrated circuits inside could be damaged. This step should first be read in its integrity; only then you should proceed with the described actions.

While performing the next step, the current drawn from the power supply shown on its ammeter should be of the order of tens of milliamps if the converter operates correctly. If you observe something different, turn off the power supply and ask the teacher to check the circuit again.

10. Supply the control circuit:
    (a) turn on the control circuit power supply;
    (b) slightly increase the current limit of the appropriate section (*Current* knob) so as the red current limiting mode indicator (*C.C.*) goes out;
    (c) set the supply voltage (*Voltage* knob) to 10 V. If the current limiting mode is activated in the course of setting (the red indicator lights up), first decrease the voltage (turn the *Voltage* knob counterclockwise) so as the red indicator extinguishes, next increase the current limit and only after that try to increase the voltage again;
    (d) after voltage is successfully set, increase the current limit by approximately the same amount that is has been set until now (at a guess).
11. Check whether the gate driver is switched off, which is indicated by the yellow light being off. Otherwise, switch it off by pushing the red button.

Setting up the oscilloscope

12. Using the oscilloscope communication software, upload to the oscilloscope the appropriate initial settings:

    [TDS224]

    - from the menu choose *File* ▸ *Open* and open the file *ustawienia_3b_przeb_tds224.sht*; choose *Offline* in the dialog that appears;
    - on the list displayed in the left panel, unfold the installed oscilloscope ▸ *Data* ▸ *Settings*;
    - in the settings file window, select its entire contents and drag them to the *Full Setup* item in the left side panel using the mouse;
    - wait for the introduction of settings on the oscilloscope to complete, which process is indicated by changes of elements on the screen (letters, numbers, curves).

    [TDS1002B]

    - switch to the *Get & Send Settings* tab;
    - click *Open* and read the file *ustawienia_3b_przeb_tds1002b.set*;
    - click *Send Settings*;
    - return to the *Screen Capture* tab.
13. Using *CH1/2/3/4 Menu* buttons on the oscilloscope, display the waveform from channel 1 and hide waveforms from all the other channels.

On the oscilloscope's screen, a constantly refreshed and stable pulse wave should be seen, which is among others indicated with the message "Trig'd" (Triggered) displayed above the graticule. If this is not the case, ask the teacher to check oscilloscope settings.

CHx Menu buttons (where x is channel number) cause toggled displaying and hiding the waveform form a given oscilloscope channel. When a given waveform is displayed, this is indicated by an arrow left of the graticule showing the zero level as well as channel symbol "CHx" under the graticule.

14. Adjust:
    - time base and trigger event position (*Sec/Div* and *Position* knobs) so that 3 to 5 periods of the u_g waveform can be seen on the screen (the trigger moment indicated with an arrow above the graticule must be located within the screen, i.e., it cannot be located at either graticule edge);
    - channel 1 gain and zero level position (*CH1 Volts/Div* and *Position* knobs) so that the waveform is clearly visible, is located at the very bottom of the screen and occupies approximately 1 division vertically.

      Short spikes or oscillations present in waveforms should be always disregarded throughout this exercise.

4.3. Converter component roles

Supplying the circuit

1. Make sure that no wire touches the load resistor, its heat sink, nor the heat sink found at the back of the converter's enclosure. This also applies to voltage probe cables. Otherwise, wire insulation could melt.

   The above conditions must be met throughout the entire exercise!

2. Supply the power circuit:
   (a) turn on the power circuit supply;
   (b) set the current limit to maximum (*Current Coarse* knob);
   (c) from the web page, obtain and write down the input voltage U_i;
   (d) slowly set the voltage to the value determined above (*Voltage Coarse* and *Fine* knobs), checking whether no constant current flow is indicated by the power supply's ammeter; in the opposite case, turn off the power supply and ask the teacher to check the circuit again.

   After performing the next step, if the converter operates correctly, the current drawn from the supply as indicated by its ammeter should be close to, but not greater than predicted for an ideal converter, equation (3.30) [for any necessary values, see Section 4.1, step 4.2/9(c) and step 2(c) above]. If anything else is observed, turn off the power circuit supply and ask the teacher to check the circuit again. In the course of the exercise, this current will reach higher values.

3. Turn on the converter in a way to ensure its operation without problems in the entire required range of the duty cycle:
   (a) switch the transistor gate driver on using the red button;

   When the converter is operating (the gate driver is on and the power input is supplied), important currents and voltages may be shown on the meters of the power supply. This results from transmission of fast disturbances while the power supply is not earth-grounded. This does not indicate incorrect circuit operation.

   (b) check whether the current limiting mode has not been activated in the control circuit power supply; if it has, increase its current limit;
   (c) set the maximum duty cycle on the function generator, i.e. 0.8;
   (d) repeat step (b);
   (e) restore the duty cycle of 0.35

Setting up voltage measurement

4. [TDS224] Display the channel 2 waveform (*CH2 Menu*). Adjust channel 2 gain and zero level position (*Volts/Div* and *Position* knobs) so that the waveform is clearly visible, is not superimposed on the u_g waveform and occupies approximately the lower 1/3 to 1/2 (not more) of the screen vertically.
5. [TDS1002B] Display the output voltage u_o on the oscilloscope without losing the image of the u_g voltage:
   (a) save the drive voltage u_g waveform in the memory of the oscilloscope:
      - push *Save/Recall*,
      - using the appropriate button beside the screen, set *Action* to *Save Waveform*,
      - select saving to oscilloscope memory, *Save To*: *Ref*,
      - set *Source* to channel 1 (*CH1*),

- select destination as Memory A, *To*: *Ref A*,
- push *Save*;

From this moment on until the end of exercise, under no circumstances should you modify the time base (*Sec/Div*) nor the triggering event position (*Horizontal Position*)! This would de-synchronize oscilloscope images relative to each other and consequently would disable their analysis during result elaboration.

(b) display the u_g waveform from the Memory A by pushing *Ref Menu* and then, using an appropriate button beside the screen, set *Ref A* to *On*;

The u_g waveform coming from the oscilloscope memory should become displayed in the background of the screen. This can be checked by slightly moving the u_g waveform coming from channel 1 using the *Vertical Position* knob.

(c) transfer the channel 1 probe so that to measure the output voltage of the converter u_o;

(d) adjust channel 1 gain and zero level position (*Volts/Div* and *Position* knobs) so that the waveform is clearly visible, is not superimposed on the u_g waveform and occupies approximately the lower 1/3 to 1/2 (not more) of the screen vertically.

Setting up current measurement

6. Configure the current probe amplifier and its connection to the oscilloscope following the short manual available at the laboratory stand. Take into account that in the worst case, the current in the circuit can reach a value equal to the quotient of the input voltage U_i [see step 2(c)] and the load resistance R_L (see Section 4.1). The amplifier's output should be connected to the oscilloscope's last channel (4 or 2 as appropriate). Obligatorily read and follow the oscilloscope configuration guidelines given in that manual.
7. Set DC coupling on the current probe amplifier.
8. Clamp the current probe around the wire that leads the inductor (not present at the moment) current i_L so that the positive current direction indicated by the arrow at the end of the probe is in line with reality (see Fig. 8).
9. Show the i_L waveform on the oscilloscope (use an appropriate *CH1/2/3/4* button) and adjust:
   - the gain along the measurement path (on the amplifier or on the oscilloscope, as described in the probe manual, not in any other way), and
   - waveform position, using the *Position* knob for the appropriate channel (on the oscilloscope),

   so that the current waveform is clearly visible from its zero level, indicated by an arrow with channel number left of the graticule, to its peak value, that it is not superimposed on other waveforms and occupies approximately the upper 1/3 to 1/2 of the screen.

Effect of components on circuit operation

10. Record the set of 3 waveforms $\{u_g; u_o; i_L\}$:
    [TDS224]
    (a) in WaveStar application, create a new sheet of the type *YT Sheet*;
    (b) drag the 3 waveforms displayed on the oscilloscope screen (u_g, u_o, i_L) from the side panel (*Local* ▸ oscilloscope designation ▸ *Data* ▸ *Waveforms* ▸ channel designation) to the *YT Sheet* created;

    Once dragged, it is sufficient to refresh waveforms using the *Refresh Sheet* button or choosing *View*, *Refresh Datasheet* from the menu.

    A waveform can be deleted from a sheet by clicking on its number left to the graticule and pressing the *Delete* key.

(c) save the datasheet, containing all the waveforms 3 together, in WaveStar format (SHT), using the *Save Datasheet* button or selecting *File* ▸ *Save Datasheet As* from the menu;

Do not use the *Save Worksheet* function, which does not save any measurement data, only names of open datasheets.

(d) write down the conversion factor setting of the current probe amplifier (see the "Current to voltage conversion" section in the manual for the probe used).

[TDS1002B]

(a) in the OpenChoice Desktop application, switch to the *Screen Capture* tab;

(b) download the screen image to the computer by clicking *Get Screen*;

(c) save the oscilloscope image using a graphic format by clicking *Save As*.

11. Insert the choke L in the circuit:
    (a) detach the current probe from the circuit;
    (b) switch the gate driver off, then turn off the power circuit supply;
    (c) remove the shorting wire from the blue screw terminal and connect the choke in its place;
    (d) place the shorting wire back in the bag in order to prevent its loss;
    (e) turn on the power circuit supply, then switch the gate driver on;
    (f) re-clamp the current probe around the wire that leads the inductor current i_L.
12. Without changing any settings on the oscilloscope nor on the current probe amplifier, record the waveform set again:

    [TDS224]

    (a) refresh the YT Sheet contents using the *Refresh Sheet* button or choosing *View* ▸ *Refresh Datasheet* from the menu;
    (b) save the datasheet in WaveStar format (SHT).

    [TDS1002B]

    (a) download the screen image to the computer by clicking *Get Screen*;
    (b) save the oscilloscope image using a graphic format.
13. Insert the capacitor C in the circuit (keep the choke inserted):
    (a) detach the current probe from the circuit;
    (b) switch the gate driver off;
    (c) to the circuit's output (u_o), in parallel to the load (according to Fig. 8, see the description in Section 4.1), connect the capacitor paying attention to its proper polarity (negative terminal is marked on its case);

    Mounting correctness must be checked by the teacher!

    (d) switch the gate driver on;
    (e) re-clamp the current probe around the wire that leads the inductor current i_L.
14. Repeat step 12.

SPDT semiconductor switch

15. Optimise current measurement path settings for the present measurement conditions:
    (a) modify the gain (on the amplifier or on the oscilloscope, as described in the probe manual) and waveform position (*Position* knob of the oscilloscope) so that they are appropriate for the presently observed values of current, whose waveform should occupy approximately the upper 1/3 to 1/2 of the screen from its zero level to its peak value;
    (b) [TDS224] write down the present conversion factor setting of the current probe amplifier;

(c) [TDS1002B] record the set of waveforms $\{u_g;\ i_L\}$ with current settings—download the image and save using a graphic format.

Special attention is required during the following step so that different circuit points are not accidentally shorted with ground connectors of oscilloscope probes.

16. * Move the voltage probes:

[TDS224]

(a) detach voltage probes (both tips and ground connectors) from the circuit;

(b) attach ground leads of both probes to the same point, the common node for the transistor (source) and the diode (cathode);

(c) attach probe tips so as to measure:

- the voltage across the diode u_D on channel 1,
- the voltage across the transistor u_T on channel 2;

(d) if needed, adjust gains and zero levels of channels 1 and 2 (*Volts/Div*, *Position*).

[TDS1002B]

(a) detach the voltage probe from the circuit;

(b) attach the probe ground to the common node for the transistor (source) and the diode (cathode);

(c) attach the probe tip so as to measure the voltage across the diode u_D;

(d) if needed, adjust the gain and the zero level of channel 1 (*Volts/Div*, *Position*) so that this waveform does not overlap the remaining two.

17. [TDS224] Record a complete set of 3 waveforms $\{i_L,\ i_D,\ i_T\}$ (* 5 waveforms $\{u_D,\ u_T,\ i_L,\ i_D,\ i_T\}$):

(a) create a new *YT Sheet*;

(b) to the *YT Sheet*, drag u_g and i_L (* u_D, u_T and i_L) waveforms, however without saving the sheet for now;

(c) without changing any settings, clamp the current probe so as to observe the diode current i_D, keeping the measurement positive direction in line with reality (see Fig. 9);

(d) download the current waveform to the computer by dragging the appropriate channel again (do not delete nor refresh the waveforms downloaded previously, do not save now); you are only allowed to change waveform colour or slightly shift it with respect to the inductor current;

(e) without changing any settings, clamp the current probe so as to observe the transistor current i_T, keeping the measurement positive direction in line with reality (see Fig. 9);

(f) download the current waveform to the software by dragging the appropriate channel again (do not delete nor refresh the waveforms downloaded previously); you are only allowed to change waveform colour or slightly shift it with respect to the currents downloaded previously;

(g) save the datasheet containing the 3 (* 5) downloaded waveforms in WaveStar format (SHT).

18. [TDS1002B] Record sets of waveforms $\{u_g,\ i_D\}$ and $\{u_g,\ i_T\}$ (* $\{u_g,\ u_D,\ i_D\}$ and $\{u_g,\ u_T,\ i_T\}$):

(a) without changing any settings, clamp the current probe so as to observe the diode current i_D, keeping the measurement positive direction in line with reality (see Fig. 9);

(b) download u_g and i_D (* u_g, u_D and i_D) waveforms and save using a graphic format;

(c) * attach the voltage probe tip so as to measure the voltage across the transistor u_T;

(d) * if needed, adjust channel 1 gain and zero level (*Volts/Div*, *Position*);

(e) without changing any settings, clamp the current probe so as to observe the transistor current i_T, keeping the measurement positive direction in line with reality (see Fig. 9);

(f) download u_g and i_T (* u_g, u_T and i_T) waveforms and save using a graphic format.

19. [TDS1002B] Hide the u_g waveform coming from the oscilloscope memory: push *Ref Menu* on the oscilloscope and set *Ref A* to *Off*.
20. Switch the gate driver off, then turn off the power circuit supply.

4.4. Electric power conversion with the buck converter

Measurement of converter characteristics

A block diagram of the measurement set-up is shown in Fig. 10 where connections to be created or modified in the way described below are drawn in black; gray lines represent existing connections that do not change.

To make exercise realisation more efficient, one person should perform step 1, while the second one should start performing steps 2–3 in parallel.

1. Using the oscilloscope communication software, introduce settings that will enable measuring the transistor current duty cycle:

   [TDS224]

   - from the menu, select *File* ▸ *Open* and open the file *ustawienia_3b_char_tds224.sht* in the next dialog box while selecting *Offline*;
   - in the file window, select all the instructions and using the mouse, drag them to the *Data* ▸ *Settings* ▸ *Full Setup* item in the left side panel.

   [TDS1002B]

   - go to the *Get & Send Settings* tab;
   - press *Open* and read the file *ustawienia_3b_char_tds1002b.set*;
   - press Send Settings.

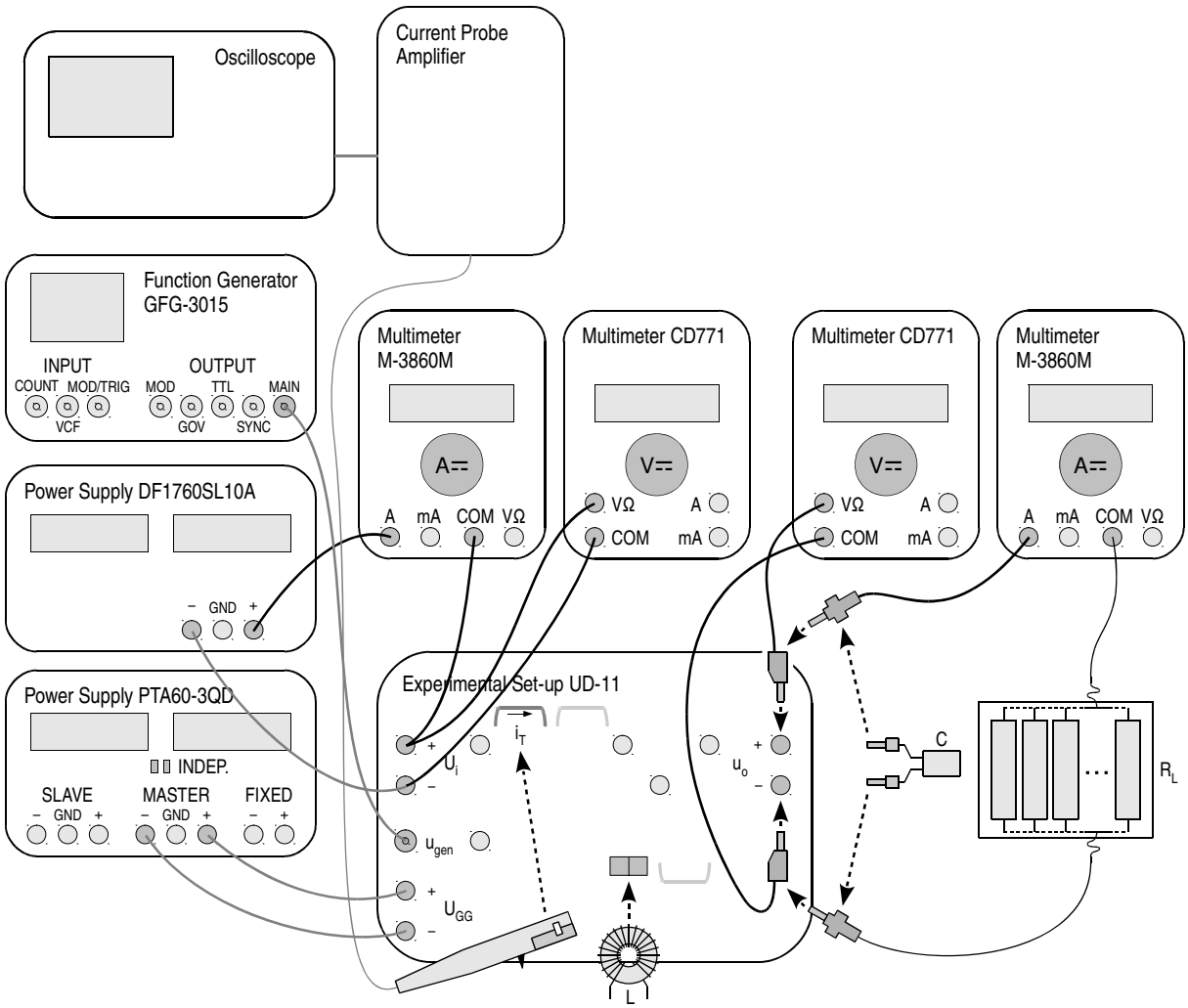

Fig. 10. Block diagram of the measurement set-up for static characteristics of the converter

2. Enable the measurement of the input and the output voltages:
   (a) in parallel to the input (U_i) and in parallel to the output (u_o), considering the way the capacitor should now be connected as shown in Fig. 10, connect two CD771 multimeters so that to enable voltage measurement;
   (b) switch the multimeters to their voltage measurement mode (V);
   (c) with the blue button, set the multimeters to the DC component measurement mode (the ⎓ symbol on the display).
3. Enable the measurement of the input and the output current:
   (a) in series with the input (U_i), i.e. between the power circuit supply and this input, and in series with the output (u_o), i.e. between this output and the receiver, considering the way the capacitor should now be connected as shown in Fig. 10, connect two M-3860M multimeters so that to enable current measurements of a few amps;
   (b) switch the multimeters to their current measurement mode considering the current value mentioned above;
   (c) with the AC/DC button, set the multimeters to the DC component measurement mode ("AC" symbol absent from the display).

   If the battery discharge indicator (a battery symbol) shows up on the meter's display, do not continue measurements but ask the teacher to replace the battery. Otherwise meter indications may become erroneous.

   Before proceeding, meter connections must be checked for correctness by the teacher.

4. Turn on the power circuit supply, next switch the gate driver on.

   Do not touch the load resistors because of the risk of scald. Once again ensure that no wires touch the resistors nor the heat sink.

5. Obtain a correct measurement of the transistor current pulse width:
   (a) change the gain in the current measurement path, in accordance with the current probe instruction manual, and possibly the waveform vertical position (*Vertical Position* knob) so that the current pulse top appears near the upper boundary of the display (it can even go a little beyond) and most of the spike visible at the beginning of the pulse is out off the display;
   (b) change the time base (*Sec/Div*) and the trigger event position (*Horizontal Position*) so that a (one) single pulse can be seen, occupying the largest possible part of the screen horizontally;
   (c) check that a relatively stable value is displayed in the right panel on the screen, in the measurement field described as *Source*: *Ch2* or *Ch4* (as appropriate), *Type*: *Pos Width* (brief distortions of this indication may happen from time to time), and that this value corresponds to the actual pulse width which should be read out from the screen using the graticule; ask the teacher for help otherwise.
6. For 7 to 15 measurement points set by the duty cycle D varying from its minimum to its maximum value possible with the generator used, i.e. from 0.2 to 0.8, write down the following measurement results:
   (a) from the oscilloscope, transistor current pulse width $t_{p(iT)}$, each time controlling the correctness of the image and (roughly) of the value displayed as in point 5 and making appropriate adjustments to the settings if necessary;

   Do not waste time for recording the waveform from the oscilloscope as it will not bring anything to result analysis which cannot be brought by simply writing down the pulse width displayed which, however, takes less time than downloading the waveform and its saving to a file.

   (b) from the multimeters, the DC component values of the input voltage U_i, the input current $I_{i(0)}$, the output voltage U_o and the output current I_o.

Similar to our theoretical analysis, we assume that the ripple in the input and the output voltages is negligible and therefore the u_i, u_o and, consequently, i_o can be considered as constant over time. It is not however possible in relation to the input current i_i; the result of multimeter measurement must therefore be denoted with the subscript "0" to clarify that it is its DC component only.

7. Set the duty cycle $D = 0.5$.

Measurement completion

8. Switch the gate driver off, next turn off the power circuit supply and next, the control circuit power supply.
9. On the oscilloscope, turn off bandwidth limiting in the current measurement channel by pushing *CH2* or *CH4 Menu* as appropriate and setting *BW Limit* to *Off* using an appropriate button right of the screen.
10. Turn off the multimeters.
11. Disconnect the current probe from the circuit.
12. Remove the choke and tighten back the screws in the terminal block. Remove the capacitor. Place the choke and the capacitor in the bag together with the bare shorting wire.
13. Disconnect the set-up.

D

Results

5. Results Processing and Analysis

5.1. Buck converter topology

Semiconductor switch

1. Based on the sets of waveforms

   [TDS224] $\{i_L, i_D, i_T\}$ (* $\{u_D, u_T, i_L, i_D, i_T\}$) recorded in step 4.3/17 as well as $\{u_g, u_o, i_L\}$ recorded in step 4.3/14:

   [TDS1002B] $\{u_g, i_D\}$ and $\{u_g, i_T\}$ (* $\{u_g, u_D, i_D\}$ and $\{u_g, u_T, i_T\}$) recorded in step 4.3/18 as well as $\{u_g, i_L\}$ recorded in step 4.3/15(c):

   (a) prove that the MOSFET and the diode act as an SPDT switch in the investigated circuit (see Refs. B and E);

   (b) determine the link between the u_g voltage and the state of the transistor (on/off).

   > [TDS224] The two sets of waveforms should be correlated based on the i_L waveform which is found in both of them.
   >
   > [TDS1002B] The three sets of waveforms should be correlated based on the u_g waveform which is found in each of them.

2. * Analyse the off-state of semiconductor devices:

   (a) from the set or sets of waveforms analysed in step 1, read out value of the voltage across the transistor u_T and of the voltage across the diode u_D in their off-state, including the signs;

   (b) justify the values read out referring to circuit topology (i.e., electrical connections obtained with the semiconductor switch being on) in a given sub-interval (see Ref. B) and to known circuit operation parameters (see steps 4.2/9 and 4.3/2);

   (c) considering the voltage values read out, does either semiconductor device forward block or reverse block? is this in accordance with its capabilities? refer to static characteristics of the main circuit (see Ref. E);

(d) could the MOSFET be inserted in the circuit in the opposite direction, i.e., with drain and source interchanged? why? (see Ref. E).

Circuit component roles

3. Determine the role of each component of the buck converter circuit:
   (a) by comparison of sets of waveforms $\{u_g, u_o, i_L\}$ recorded in steps 4.3/10 (without passive components), 12 (with choke) and 14 (with choke and capacitor) state what the effect of inserting the semiconductor switch, the choke and the capacitor is;
   (b) what role may therefore be assigned to each of the above components (see Ref. B and Section 3)?
4. * Analyse conditions in which the passive components operate:
   (a) based on known circuit component values (Section 4.1) and known switching frequency (step 4.2/9) state whether conditions are met for inductor and capacitor to properly fulfil their tasks, i.e. (3.14) and (3.24)?
   (b) state and justify whether waveforms analysed in step 3 prove that the considered relationships express indeed conditions for inductor and capacitor proper operation.
5. Based on the set of waveforms $\{u_g, u_o, i_L\}$ recorded in step 4.3/14:
   (a) read out the following values:
      - output voltage U_o,
      - DC component of inductor current $I_{L(0)}$,
      - * inductor current ripple amplitude ΔI_L;

      [TDS224] take into account the current probe conversion factor written down in step 4.3/10(d);
   (b) justify the values obtained by referring to known circuit component values (Section 4.1) and known circuit operation parameters (steps 4.2/9 and 4.3/2; see Ref. B, and Section 3.2.d for a relationship for the DC inductor current).

5.2. Circuit characteristics and transistor's effect

Obtaining characteristics with respect to the controlling quantity

1. Based on the results of measurements carried out in step 4.4/6, for each measurement point calculate (see Section 3.3):
   (a) actual (i.e. manifested in the power circuit, and thus in the transistor current, and not the one delivered from the generator to the input of the control circuit) duty cycle D, from the measured transistor current pulse duration $t_{p(iT)}$ and the known repetition frequency f_s (see step 4.2/9);
   (b) average input power P_i, from the appropriate current and voltage measured (assuming the voltage is constant over time);
   (c) average output power P_o, from the appropriate current and voltage measured (assuming the voltage is constant over time);
   (d) efficiency η, from its definition (see Manual 0, Ref. B),
   (e) voltage conversion ratio K_U , from its definition (3.40);
   (f) * current ratio $I_{i(0)} / I_o$.

   Gather measurement and calculation results in Table 1.
2. For each duty cycle value D, calculate and add to Table 1 (see Section 3.3):
   (a) voltage conversion ratio for the ideal (lossless) converter $K_{U(id)}$, from the analytical formula;
   (b) relative difference in voltage conversion ratio between the real and the ideal circuit $(K_U - K_{U(id)}) / K_{U(id)}$, based on the results from steps (a) and 1(e);
   (c) * $K_U / K_{U(id)}$ ratio, based on the results from steps (a) and 1(e);
   (d) * the ratio of the measured current ratio $I_{i(0)} / I_o$ to its theoretical value, based on the results from step 1(f).
3. For a dense set of duty cycle D values over its full possible range of [0; 1], so that it is possible to subsequently plot a curve covering the entire range from 0 to 1 and giving the impression of a smooth curve, calculate again the voltage conversion ratio of the ideal converter $K_{U(id)}$. Gather these results in a separate Table 2.

Results analysis

4. Based on data from Table 1, plot the characteristic of efficiency η as a function of duty cycle D.
5. Analyse the obtained curve:
   (a) is the obtained efficiency level high or low as compared to linear-mode circuits (see Manual 0, Refs. B and E)?
   (b) how does the efficiency change with the duty cycle?
   (c) * if we assume that power losses are mainly introduced by the transistor (determining whether it is indeed true, would require a much wider program of measurements), would the shape of the measured characteristics demonstrate the dominance of dynamic or static power loss, or a comparable contribution of both (see Section 3.3)?
6. Illustrate the conversion characteristics of the circuit under investigation in combination with the ideal converter characteristics (all of the below as functions of the duty cycle D):
   (a) in one graph, include two characteristics of the conversion ratio, the measured one K_U, based on Table 1, and the ideal converter one $K_{U(id)}$, based on Table 2;
   (b) in a separate graph, based on Table 1, present the relative difference in voltage conversion ratios $(K_U - K_{U(id)}) / K_{U(id)}$ as a function of the transistor current duty cycle D;
   (c) * in a separate, single plot, based on Table 1, present the proportion of the voltage conversion ratios $K_U / K_{U(id)}$ and the efficiency η.

7. Analyse the course of the experimental characteristic in comparison with the theoretical one:
   (a) what is the sign (in plus or in minus) and the order of magnitude of the discrepancy between them in absolute numbers [graph of step 6(a) and Table 1] and in relative numbers [graph of step 6(b) and Table 2]?
   (b) does the above discrepancy vary with the duty cycle? in what way?
   (c) relate the above observation to the trend of the efficiency characteristic $\eta = f(D)$; is there any regularity noticeable in this respect (i.e. characteristic trends), i.e. a correlation between the efficiency and the discrepancy between the voltage conversion ratios for the real and for the ideal converter, visible over the entire value range of D?
   (d) * refine the conclusion of sub-step (c) by performing a quantitative analysis: based on the graph produced in sub-step 6(c), determine whether, in accordance with theoretical predictions, the relationship (3.52) holds.
8. * Analyse the relationship between the converter currents:
   (a) based on data from Table 2, plot the proportion of the measured current ratio $I_{i(0)} / I_o$ to this ratio theoretical value (specify what this value is);
   (b) based on the graph obtained, determine whether, in accordance with theoretical predictions, the relationship (3.28) holds and whether it is true for a real (lossy) converter.

Transistor power loss minimisation

9. Let us assume we want to increase the efficiency of the converter by reducing both the static $P_{T,stat}$ and the dynamic power loss $P_{T,dyn}$ in the transistor at least by a factor of two. What criteria should we apply in search for a better suited transistor? Base on eqs. (3.33) and (3.43) (see also Ref. F and Manual 3^A, Ref. D). Express these criteria numerically in the form of inequalities based on the datasheet of the transistor used in the investigated converter.
10. * If changing the transistor were not an option, what other action influencing its operation could be taken to increase the efficiency? Base on results from part A of this exercise.

E

Information

6. Expected Report Contents

1. Waveforms of switch branch currents (* and voltages) across semiconductor devices, and the driving waveform, together with inductor current, labelled with current/voltage conversion factors of the current probe (for TDS224), according to step 5.1/1
   [TDS224] [i.e., $\{i_L, i_D, i_T\}$ (* $\{u_D, u_T, i_L, i_D, i_T\}$) and $\{u_g, u_o, i_L\}$ sets]
   [TDS1002B] [i.e., $\{u_g, i_D\}$, $\{u_g, i_T\}$ (* $\{u_g, u_D, i_D\}$, $\{u_g, u_T, i_T\}$) and $\{u_g, i_L\}$ sets]
2. Waveform analysis with respect to the SPDT switch action, according to step 5.1/1
3. * Off-state voltage values across semiconductor devices with their justification, including formulae used and calculations made, together with references to properties of these devices, according to step 5.1/2
4. Waveforms of driving voltage, output voltage and inductor current for three sets of converter components, put together on one page side by side or one under another, and their analysis, according to step 5.1/3
   (i.e., $\{u_g, u_o, i_L\}$ sets for the cases without passive components, with choke added and with capacitor added)
5. * Conditions for proper operation of passive components given in numerical form, their comparison to values of components used and a reference to measurement results, according to step 5.1/4
6. Voltage and current values read out of oscilloscope images and their justification, with formulae used and calculations made, according to step 5.1/5
7. Table with calculation results of experimental efficiency and voltage conversion ratio (* current ratio) characteristics, according to steps 5.2/1—2
8. Table with calculated points along the theoretical conversion characteristic, according to step 5.2/3
9. Efficiency characteristic plot and its analysis, according to steps 5.2/4—5
10. Plots of the experimental conversion characteristic combined with the theoretical one, of the difference in voltage conversion ratios (* as well as of the proportion of

voltage conversion ratios combined with the efficiency) and their analysis, according to steps 5.2/6—7

11. * Plot and analysis of the proportion of the current ratio measured to its theoretical value, according to step 5.2/8
12. Numerically expressed transistor search criteria for reduced power loss, according to step 5.2/9
13. * Proposal of another circuit modification permitting increasing efficiency, according to step 5.2/10

7. Required Knowledge

7.1. Prerequisites

- Switched mode of circuit operation: a typical control signal waveform, duty cycle, switching period and frequency.
(see Ref. B; Manual 0, Ref. B; Section 2.2)
- Buck DC/DC converter operating principle: schematic, the SPDT switch and its operation, circuit reduced topology in the two sub-intervals of switching period, choke current waveform
(see Ref. B and Manual 0, Ref. B)

7.2. Test scope

1. Switched mode of circuit operation: a typical control signal waveform, duty cycle, switching period and frequency.
(see Refs. B and C; Manual 0, Ref. B; Section 2.2)
2. Advantages and drawbacks of different converter types: electro-mechanical, linear-mode electronic and switched-mode electronic.
(see Manual 0, Refs. B and E)
3. Buck DC/DC converter: schematic (with an ideal switch and with semiconductor switches), SPDT switch and its operation, role of either passive element. Reduced circuit topology in two sub-intervals of switching period. Inductor, transistor and diode current waveforms synchronised with switch driving signal (including specific voltage values and their link to circuit operating conditions).
(see Ref. B and Manual 0, Ref. B)
4. Definitions of efficiency and voltage conversion ratio. Experimental and theoretical conversion characteristics for the ideal (lossless) buck converter (formula and plot). Efficiency characteristics of the buck converter (plots), considering static and dynamic transistor power loss; effect of transistor parameters. Experimental efficiency characteristic; experimental characteristic of the relative difference in the voltage conversion ratio between the real and the ideal converters as a function of duty cycle; link between these characteristics including the theoretical relationship (a formula for the voltage conversion ratio containing the efficiency).
(see Section 3.3; Ref. B; Manual 0, Ref. B; report)
5. Favourable and unfavourable consequences of increasing switched-mode converter operating frequency; resulting requirements related to semiconductor devices.

Reasons for power MOSFET popularity.
(see Section 3.3.f, report)

When results included in your report are concerned, restrict to the qualitative aspect (character of relationships) and indicatory values.

8. References

[1] Benda V., Gowar J., Grant D. A.: *Power Semiconductor Devices: Theory and Applications.* Wiley, 1999. ISBN 0-471-97644-X.

[2] Erickson R. W., Maksimović D.: *Fundamentals of Power Electronics. Second Edition.* Springer, 2001. ISBN 0-792-37270-0.