Politechnika Łódzka
Katedra Mikroelektroniki i Technik Informatycznych
90-924 Łódź, ul. Wólczańska 221/223, bud. B18
tel. 42 631 26 28 faks 42 636 03 27 e-mail secretary@dmcs.p.lodz.pl
http://www.dmcs.p.lodz.pl

POWER DEVICES AND SYSTEMS LABORATORY

Exercise 5^{A}

Bipolar Junction Transistor

Static Characteristics of Power Transistors

Indicatory work plan

15′	30′	45′	1^{h}	1^{h}15′	1^{h}30′	After Class
5.1	5.2/1–7		5.2/8–13	5.3/1–7	5.3/8–13 5.4	6

Exercise and manual elaborated by
Łukasz Starzak
Parts C and D (ver. 5.5) translated by
Henryk Błasiński

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Exercise Introduction

1. Exercise Aim and Plan

The aim of this exercise is to investigate and compare static properties of different power transistors: BJT (discrete and Darlington), MOSFET and IGBT. This will enrich the understanding of why all these devices are still present on the market, each one in its own area of application. Using a special power device curve tracer, appropriate characteristics will be recorded. From the recorded images, data for the on-state will be extracted and used to calculate power losses for different load values. Lacking parameters will be read out from device datasheets. Based on results obtained, a comparison of the different devices will be made with respect to the possibility of their application, depending on the load current as well as on the main circuit power loss and the drive power requirements.

The exercise is also an occasion to investigate more thoroughly the power bipolar junction transistor (BJT). This is because its advantages are particularly apparent when static properties of its main circuit are concerned.

Some information about physical mechanisms present in semiconductor devices, especially conduction mechanisms, covered in Refs. H, I and J of Manual 0, will be useful.

2. Power Bipolar Junction Transistors

2.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
A	Ben	6, 6.1, 6.2.1, 6.2.2, 6.3.2	2.1, 2.2, 2.3, 2.4		
B	Ben	6.5	2.5		

Also read again: Manual 0, Ref. H, 3.1.2.

3. Application Significance of Transistor Static Parameters

3.1. Main parameters of power semiconductor devices

3.1.a. Power semiconductor device key absolute maximum parameters

The Bipolar Junction Transistor was the first transistor for which a high-voltage structure was invented. It had several drawbacks, which led to the invention of the power MOSFET. The disadvantages of the latter were in turn an inspiration for development of better (in certain respects) devices such as the IGBT.

It appears however that MOSFETs and BJTs are still present on the market. It follows from the simple fact that engineers still want to apply them in their designs. Disregarding the role of psychological factors—such as habits and resistance to changes—the conclusion can be drawn that older devices must still be better in certain areas. One has only to determine what areas they are.

When talking about power semiconductor device application areas, this issue may be considered from the application point of view (in what circuits a given device can be useful, but this would make it necessary to consider the principles of operation of these circuits) or from the device point of view (what requirements for parameter values a given device can fulfil). Three main, easy to compare absolute maximum (maximum admissible) parameters are usually considered:

1) voltage (voltage capability),
2) current (absolute maximum),
3) frequency (maximum switching).

It should always be remembered that in the majority of applications the power semiconductor devices are considered as switches, i.e. elements switched with a given frequency between the off-state (blocking) and the on-state (conducting).

3.1.b. Frequency

The maximum working frequency of a semiconductor switch results from its dynamic parameters. They are, first of all, the turn-on time and the turn-off state and (as a consequence) the energy dissipated during turn-on and during turn-off. Dynamic phenomena and parameters are not the subject of this exercise.

The different transistors investigated in this exercise can be briefly characterised in this respect as follows:

— **MOSFETs**, as unipolar devices, are much faster than all the bipolar devices;
— **IGBTs** practically turn on as fast as MOSFETs but are characterised with a particularly long and energetically unfavourable turn-off (the current tail) even though this drawback can presently be successfully minimised;

— **BJTs**, as a strictly bipolar device, is characterised with relatively long switching times;

— **the BJT darlington** turns off most slowly.

3.1.c. Voltage

The voltage capability of power semiconductor devices results from parameters of the lightly-doped layer included in their structure. They determine the breakdown voltage of the junction across which the high voltage is sustained.

In this respect, technological possibilities are similar for each of the considered transistors. Differences arise from physical-electrical limitations:

— for unipolar transistors any improvement in voltage capability is connected with an increase in the on-state resistance (which is a consequence of decreasing the dopant concentration and increasing the length of the lightly-doped layer);

— for bipolar devices any improvement in voltage capability is connected with an increase in switching times (which is a consequence of increasing the lightly-doped layer length and increasing the excess carrier lifetime with the intention of reducing the on-state resistance), and for the BJT, additionally, with a decrease in current gain (a decrease of the transport coefficient α_t due to the lengthening of carriers' path).

As a consequence, it is commercially profitable to manufacture transistors with voltage capabilities of the following orders of magnitude:

— for MOSFETs: up to hundreds of volts;

— for BJTs (discrete): up to kilovolts but only for weak currents while up to tens (or a hundred) volts for strong currents;

— for IGBTs: up to one kilovolt and more.

3.1.d. Current

The maximum current that a given element can conduct is related to the capability of heat conduction (the heat being a result of power dissipation caused by the current flow) out of the semiconductor structure. A more intensive energy dissipation needs bigger, more enduring and more complex a case. It may be also necessary to apply additional cooling elements such as heat sinks, heat sink forced cooling (fans, fluid circulation) and even semiconductor forced cooling (micro-channels with cooling fluid realised in the semiconductor substrate). This of course affects the cost of device application.

Thus, under the concept of current capability, there is in fact the issue of power loss hidden (see Exercise 1). The total power loss in a device is made up by the main circuit power loss P_{main} and the drive circuit power loss P_{drv}:

$$P_{\text{tot}} = P_{\text{main}} + P_{\text{drv}} \tag{3.1}$$

Under assumption that the energy dissipated in the drive (e.g. base) circuit is much less than the energy dissipated in the main (e.g. collector) circuit, the power loss in a device in the static on-state equals

$$P_{\text{main}} = I_{\text{o}} \cdot U_{\text{on}}(I_{\text{o}}, X_{\text{in}}) \tag{3.2}$$

where I_{o} is the load current flowing through this device main circuit and U_{on} is the voltage across its main terminals resulting from the current flowing.

The on-state voltage U_{on} depends mostly on the main current but, to some degree, also on the driving (controlling) quantity X_{in}. Depending on the particular device, the driving quantity (in a static state) may be the input current I_{in} or the input voltage U_{in}. As the load is normally forced by

the external circuit, it is the on-state voltage U_{on} that constitutes the main indicator of a device's application value.

Assume that the current flowing through a transistor has a pulse waveform. This means that the transistor is conducting for some part t_{p} (the pulse width) of the switching period T_{s} and is blocking for the remaining part. The related pulse ratio is

$$D = \frac{t_{\mathrm{p}}}{T_{\mathrm{s}}} \tag{3.3}$$

Assume also that the off-state power loss can be neglected as compared to the on-state power loss. As far as dynamic power losses are concerned, we have already assumed above that they are neglectable.

Under the above assumptions the instantaneous power loss will have a pulse waveform with a pulse width equal t_{p} and an amplitude expressed with Eq. (3.2). The resulting main circuit average power loss is, by definition,

$$P_{\mathrm{main}} = \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} p_{\mathrm{main}}(t)\,\mathrm{d}t = \frac{1}{T_{\mathrm{s}}} \left(\int_{t_{\mathrm{p}}} I_{\mathrm{o}} U_{\mathrm{on}}\,\mathrm{d}t + \int_{T_{\mathrm{s}}-t_{\mathrm{p}}} 0\,\mathrm{d}t \right) = \frac{1}{T_{\mathrm{s}}} I_{\mathrm{o}} U_{\mathrm{on}} t_{\mathrm{p}} = D I_{\mathrm{o}} U_{\mathrm{on}} \tag{3.4}$$

Not only the macroscopic power (considered for the whole device as one object) but also the microscopic power is an issue. It cannot be allowed that any fragment of the semiconductor structure is overheated. This aspect makes it necessary to consider the power density

$$p_v = \frac{\Delta P}{\Delta V} = J^2 \rho \tag{3.5}$$

to be considered, where $\Delta V \to 0$ is the volume of the considered structure segment, inside which a certain amount ΔP of the total power is generated, J is the current density inside this segment and ρ is the resistivity inside this segment resulting from carrier concentration.

If decreasing the resistivity is not possible, then the power density must be minimized by decreasing the current density. Under the assumption that the structure is homogenous and that the current flow is uniform, this current density is

$$J = \frac{I_{\mathrm{o}}}{A} \tag{3.6}$$

where I_{o} is the total current conducted in the device (its main circuit) and A is the total cross-section area (perpendicular to the direction of current flow). However, increasing the silicon wafer area can be economically ineffective as it raises the cost of the wafer itself and also that of the case that must be replaced with a larger one.

3.2. Drive criterion

3.2.a. Drive power

Until now, we only considered parameters related to the main circuit. However, the drive (control) mechanism and the power necessary to control a device (the drive power) are also important factors influencing the application value of power semiconductor devices.

As we know, power transistors may be controlled using two mechanisms: current control or voltage-charge control (see Manual 0, Ref. H). We will now describe them both from the quantitative point of view. Assuming that the drive current source is ideal, the drive power is equal to the power loss in the transistor's input circuit is

$$p_{\mathrm{drv}} = i_{\mathrm{in}} u_{\mathrm{in}} \tag{3.7}$$

where i_{in} is the current in the input circuit (drive terminal current), u_{in} is the input voltage (the voltage between the drive and the common terminal).

3.2.b. Current control

It follows from the principle of current control that the drive current flow is continuous, so the power loss in the on-state is constant and equals

$$P_{\mathrm{drv}} = I_{\mathrm{in}} U_{\mathrm{in}} \tag{3.8}$$

In the specific case of BJT,

$$P_{\mathrm{drv}}(I_{\mathrm{C}}, I_{\mathrm{B}}) = I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) \tag{3.9}$$

To induce a pulse main current i_{o}, the drive signal i_{B} must also be a pulse waveform. The instantaneous power is the drive circuit will therefore have a pulse waveform, too, and its amplitude will be expressed with Eq. (3.9). Assuming that a zero base current is applied to keep the transistor in the off-state, the average drive power is

$$\begin{aligned} P_{\mathrm{drv}}(I_{\mathrm{C}}, I_{\mathrm{B}}) &= \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} p_{\mathrm{drv}} \mathrm{d}t = \frac{1}{T_{\mathrm{s}}} \left(\int_{t_{\mathrm{p}}} I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) \cdot \mathrm{d}t + \int_{T_{\mathrm{s}} - t_{\mathrm{p}}} 0 \cdot \mathrm{d}t \right) = \\ &= \frac{t_{\mathrm{p}}}{T_{\mathrm{s}}} \cdot I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) = D \cdot I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) \end{aligned} \tag{3.10}$$

Just as in the case of the power loss in the main circuit, the increased power consumption in the dynamic states has been neglected. This results in an under-estimation of power that becomes greater with switching frequency.

3.2.c. Voltage-charge control

In the second case, the flow of current that charges the input capacitance of the device is always variable. Principally, it has the form of pulses appearing during turn-on and during turn-off. The average drive power is

$$P_{\mathrm{drv}} = \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} p_{\mathrm{drv}} \mathrm{d}t = \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} i_{\mathrm{in}} u_{\mathrm{drv}} \mathrm{d}t \tag{3.11}$$

The forced drive voltage has a certain constant value equal to the steady-state input voltage U_{in}. The input current i_{in} is only drawn from the source in the turn-on time interval $t_{on(G)}$ (as considered with respect to the gate circuit). Thus,

$$P_{drv} = \frac{U_{in}}{T_s} \int_{t_{on(G)}} i_{in}(t)\mathrm{d}t \tag{3.12}$$

The integral of current is nothing else but the charge. The charge delivered to the transistor's gate during the turn-on time interval $t_{on(G)}$ is called the total gate charge $Q_{G(tot)}$. Using this quantity, the Eq. (3.12) may be expressed in the form of

$$P_{drv} = \frac{U_{in}}{T_s} \cdot Q_{G(tot)} = Q_{G(tot)} U_{in} f_s \tag{3.13}$$

where f_s is the switching frequency.

In the particular case of the MOSFET,

$$P_{drv}(I_D, U_{GS}, f_s) = Q_{G(tot)}(I_D, U_{GS}) \cdot U_{GS} \cdot f_s \tag{3.14}$$

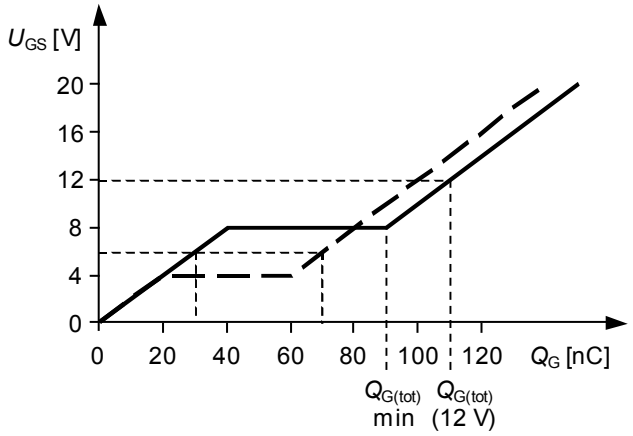
while for the IGBT,

$$P_{drv}(I_C, U_{GE}, f_s) = Q_{G(tot)}(I_C, U_{GE}) \cdot U_{GE} \cdot f_s \tag{3.15}$$

3.2.d. Total gate charge value

The total gate charge may be given in transistor's datasheet as a number. However, it should be taken into account that it is a clearly ascending function of the drive voltage U_{in} (i.e. U_{GS} or U_{GE}) and also an ascending function of the main current I_o (i.e. I_D or I_C). For given values of these quantities, the value of $Q_{G(tot)}$ can only be read out from the so-called gate charge characteristic.

Fig. 1 presents an exemplary image of this characteristic for a MOSFET transistor. For example, for a voltage U_{GS} of 12 V we can read out the total charge $Q_{G(tot)}$ = 110 nC.



Rys. 1. An exemplary gate charge characteristic used to determine the total gate charge $Q_{G(tot)}$ value

The dependence on the output current is often neglected in the gate charge characteristic as a minor factor. If the I_o value for which the characteristic was obtained is considerably greater than the one appearing in the transistor's real working circuit, this may result in a readout of $Q_{G(tot)}$ from the first rising section of this characteristic (see the case for U_{GS} = 6 V in Fig. 1). However, it follows from the principle of the method used to obtain this curve that the transistor is turned-on only at the right end of the horizontal section. For this reason, the charge delivered during turn-on $t_{on(G)}$ cannot

be less than the value that corresponds to this point. In the considered example it is $Q_{G(tot)min}$ = 90 nC.

Had the characteristic been measured for the proper, lower value of I_o, the horizontal section would have been found at a lower level (see the dashed curve), so that the readout would have been made from a point on the second rising section, $Q_{G(tot)}$ = 70 nC. If the characteristic for the lower current is not known, $Q_{G(tot)} = Q_{G(tot)min}$ = 90 nC should be assumed because this way, no error of drive power P_{drv} under-estimation is made. The value of 30 nC, which would result from a readout made in the point of intersection lying on the first rising section, is unacceptable as totally unreal.

C

Experiment

4. Measurement Set-up

4.1. Power semiconductor device curve tracer

4.1.a. General description

Measurements are carried out with the Tektronix 576 curve tracer. Fig. 2 presents a simplified diagram of this device, while Fig. 3 describes its operating principle. Both diagrams correspond to the configuration used throughout this exercise, appropriate for measurement of output characteristics of a BJT with the base driven by the current generator. There is only a slight modification In the case of MOSFET and IGBT:

- the step generator becomes a voltage pulse generator (u_{GS} or u_{GE} as appropriate),
- the tags B (base) should be replaced with G (gate),
- for MOSFET, the tags C (collector) should be replaced with D (drain), and E (emitter) should be replaced with S (source).

The operating principle of the curve tracer remains unchanged irrespectively of the type of the semiconductor device used. The curve tracer generates an appropriately varying voltage between the power circuit terminals and a correspondingly varying drive current or voltage. This results in displaying on the screen (which has the same operating principle as an analogue oscilloscope) of the on-state output characteristics of the device under test. (It is also possible to measure other characteristics such as the transfer, input or off-state output characteristic.)

Basic functions of the curve tracer, which will be used in this exercise, have been described in the abridged user's manual available at the laboratory stand. Before using any of the switches and dials it is obligatory to familiarise with its description in the manual. In order to facilitate device operation, knobs and switches have been put together into 4 groups (A, B, C and D), as presented in the figure on the cover page of the additional manual. We shall be referring to those group names and numbers in further sections of this laboratory manual.

4.1.b. Main (collector) circuit

The main circuit of the device under test is connected to the sine wave generator u_{CC} (see Fig. 2). For the case of an NPN BJT testing, the u_{CC} waveform is full-wave rectified [see Fig. 3(a)]. As a result, the voltage potential at the collector cyclically increases till reaching its maximal value U_{CCm} after which it decreases to zero [see Fig. 9(b) where arrows indicate the motion of the operating point forced by the generator voltage changes, marked in the same manner as in Fig. 9(a)].

The maximal collector voltage U_{CCm} is set by the user with the *Max Peak Volts [A1]* switch (range selection) and the *Variable Collector Supply [A3]* knob (fine adjustment in percentage of the range). This can be expressed with the formula

$$U_{CCm} = \textit{Variable Collector Supply} \times \textit{Max Peak Volts} \tag{4.1}$$

Warning!

Any change of the *Max Peak Volts* setting can only be made when the *Variable Collector Supply* knob is set to zero! Otherwise you risk supplying high voltage to the collector, which may damage the device under test.

The variable loading resistor R_{obc}, whose value is selected with the *Max Peak Power [A1]* knob, is responsible for limiting power losses in the device under test ($P_C = I_C \cdot U_{CE}$). When the collector current flows, a part of the u_{CC} voltage appears across this resistor, so the maximal value of the U_{CE} voltage is lower than the maximal generator voltage U_{CCm}. The observed characteristics are thus limited by the collector circuit load line with the inclination of $1/R_{obc}$. The power selected with the *Max Peak Power* knob corresponds to the point in the middle of this line if the amplitude U_{CCm} is equal to the full range of *Max Peak Volts* (*Variable Collector Supply [A3]* knob set to 100%); in other points and for lower amplitudes the dissipated power is always smaller.

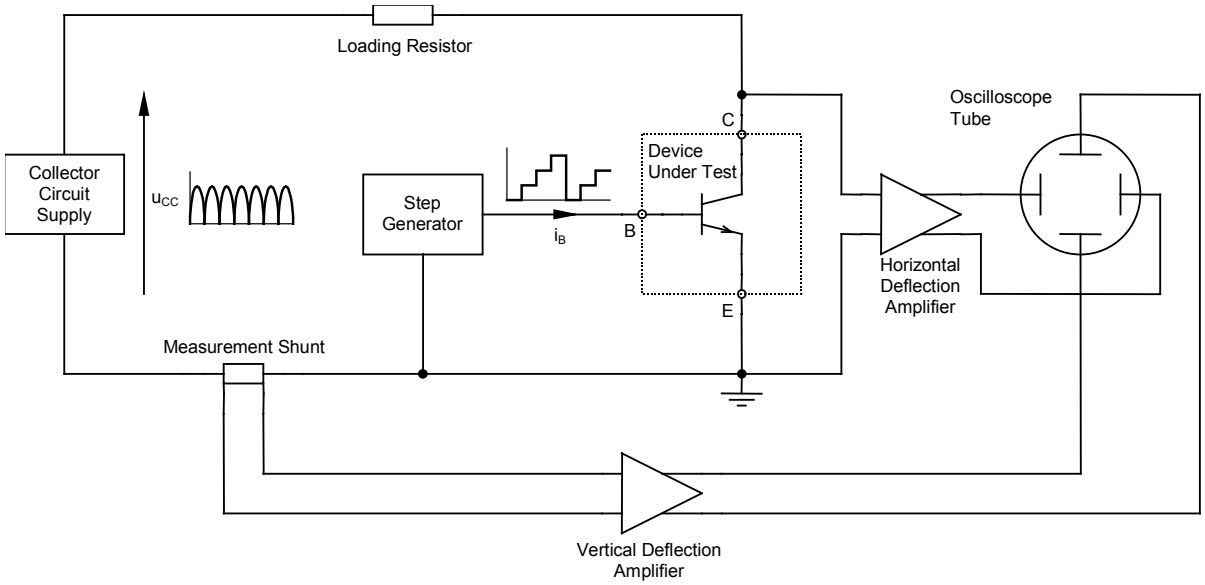


Fig. 2. Simplified diagram of the measurement circuit of the Tektronix 576 curve tracer (configuration for NPN BJT output characteristics measurement)

4.1.c. Drive (base) circuit

The base of the transistor is driven from the step waveform generator. As a result during each consecutive period of the sinusoidal collector voltage waveform, the base current takes a different value [see Fig. 3(a)], which allows plotting a family of curves for different base current I_B values [Fig. 3(b)]. A single curve (characteristic branch) of this family is plotted during each period of the u_{CC} voltage.

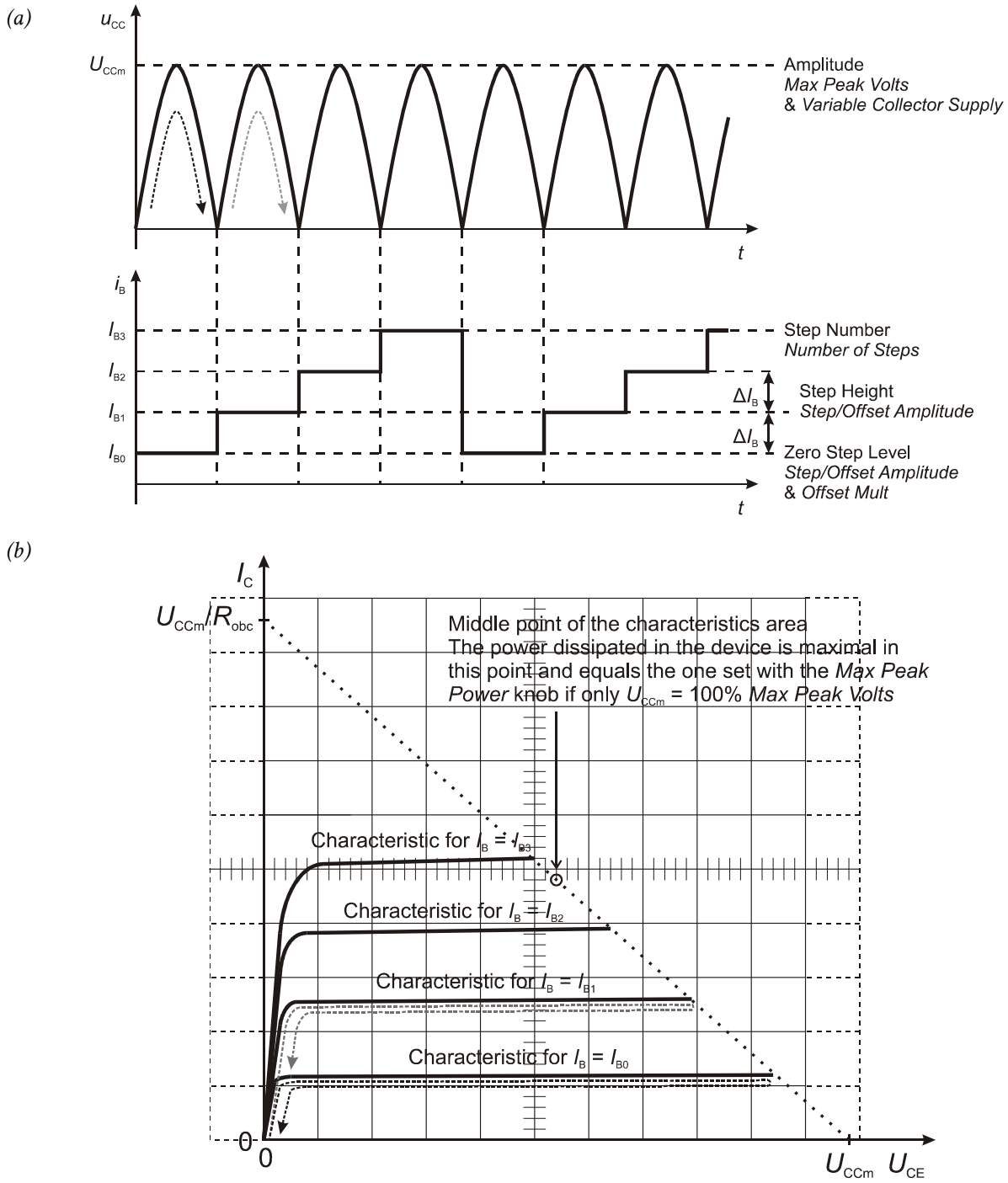


Fig. 3. Curve tracer operation during output characteristics measurements of an NPN BJT: (a) collector circuit generator and step generator waveforms (basic parameters as well as corresponding curve tracer knobs and switches have been tagged); (b) the image generated on the display (the motion of the operating point has been marked in accordance with Fig. (a) for the two first periods of the collector generator)

The number of branches (not including the always displayed zero branch) is set by the user with the *Number of Steps [B1]* switch. The base current step ΔI_B (or the height of each step) is set with the *Step/Offset Amplitude [B2]* switch.

The level of the zero step of the base current I_{B0} (corresponding to the zero-th branch of the characteristics) can be:

- zero, if the button *Zero* is pressed in the *Offset [B4]* group,

- set with the *Offset Mult [B3]* knob, if the *Aid* button is pressed in the *Offset* group.

The *Offset Mult [B3]* knob is scaled not in amperes but in multiples of the step size ΔI_B (*Step/Offset Amplitude* knob), hence

$$I_{B0} = \textit{Offset Mult} \times \textit{Step/Offset Amplitude} \tag{4.2}$$

The formula for the base current corresponding to the n-th branch of the characteristics follows from the above equation:

$$\begin{aligned} I_{Bn} &= I_{B0} + n \times \textit{Step/Offset Amplitude} = \\ &= \textit{Offset Mult} \times \textit{Step/Offset Amplitude} + n \times \textit{Step/Offset Amplitude} = \\ &= (n + \textit{Offset Mult}) \times \textit{Step/Offset Amplitude} \end{aligned} \tag{4.3}$$

If in the *Offset [B4]* group the *Zero* button is pressed, then *Offset Mult* = 0 irrespectively of the actual setting of this knob.

4.1.d. Oscilloscope circuit

The visualisation process is identical to that of an ordinary analogue oscilloscope. The collector-emitter voltage U_{CE} is connected to the input of the horizontal deflection amplifier of the oscilloscope tube (gain adjustment is done via the *Horizontal Volts/Div [C7]* knob). The voltage across the measurement shunt, proportional to the collector current I_C, drives the vertical deflection amplifier (gain adjustment via the *Vertical Current/Div [C1]* knob).

As a result of the coordinated action of the collector power supply, the step function generator and the oscilloscope circuit, on the curve tracer display a family of output characteristic curves $I_C = f(U_{CE})$ of the transistor under test is plotted as shown in Fig. 3(b).

4.2. Saving results with the digital camera

4.2.a. Taking pictures

At every step of the exercise where it is obligatory to record observed characteristics, a picture should be taken of the curve tracer display including the gain settings displayed on the right. This is done with a separate digital camera. At the end of the laboratory session all pictures should be copied to the team's account and erased from the camera.

In order to avoid blurred images, they have to be taken using the self-timer. This function is turned on with the ◄ button, afterwards you should choose *On* and accept with the ↵ button. After taking each picture the self-timer automatically turns off.

In order to obtain sharp images, one needs to first press the shutter button half way and wait for the camera to set the focus, which is indicated by the "AF" tag with a green dot in the upper part of the display. Only then the shutter button can be pressed all the way.

The quality of the acquired image can be checked in the image preview mode, which is entered by pressing the ▶ button. The *W/L* button (magnifying glass) allows zooming the image on the screen.

Reflections of bright objects may appear in the image of the curve tracer screen that make future plot analysis impossible. In such a case, one may hold a dark screen behind the camera (available in the laboratory).

4.2.b. Preparing for image acquisition

Before taking the first picture it is necessary to:

1. Fasten the camera to the tripod.
2. Turn on the camera.
3. Set the image resolution to 1024×768 (change the operating mode to the 'green camera', press the *MENU* button, select *Image mode* with ▲▼ and accept with ↵, select *PC screen* (1024), accept, turn off the menu with the *MENU* button).
4. Turn on date imprint (mode knob into the *SETUP* position, select *Date Imprint* with ▲▼ buttons, continue by pressing the ► button, select *Date and time*, accept with the ↵ button, return to the main menu by pressing ◄).
5. Select the *Sunset* program (mode knob into the *SCENE* position, press the *MENU* button, select the *Sunset* option with ▲▼◄► buttons, accept with the ↵ button).
6. Turn off the flash (press the ▲ button, select the crossed out flash symbol with ▲▼ buttons and accept with the ↵ button).

4.2.c. Transfer to PC

In order to download images onto the PC, it is necessary to:

1. Connect the camera to the PC via the USB cable.
2. Wait for the successful device installation message box to appear.
3. If a window entitled "Dysk wymienny" is displayed, click on *Otwórz folder, aby wyświetlić pliki*. Otherwise it is necessary to open *My Computer*, locate the drive letter that corresponds to the digital camera (it is usually labelled as "Dysk wymienny") and open this drive.
4. Copy the recorded images from the DCIM\xxxNIKON folder to a folder in the team's account.
5. Disconnect the camera from the PC.

6. Delete the images from the camera (press the ▶ button, then *MENU*, select *Delete*, press ▶, select *Erase all images*, press ▶, select *Yes*, accept ↵, press ▶ again).

5. Measurements

5.1. Preparation of the measurement set-up

Devices under test

Measurements are performed on power transistors listed in Table 1. As can be seen, they have been selected so that their parameters are very similar. Detailed data for these devices can be found in datasheets appended to this laboratory manual.

Table 1. Transistors tested during the exercise and their rated parameters

Symbol	Transistor Type	Rated Current (for the case temperature of 25 °C)		Rated Voltage		Maximum Drive Current or Voltage	
BU1508AX	BJT discrete	I_C	8,0 A	U_{CEO}	700 V	I_B	4 A
BU808DFI	BJT darlington	I_C	8,0 A	U_{CEO}	700 V	I_B	3 A
IRFB9N60A	MOSFET	I_D	9,2 A	U_{DSS}	600 V	U_{GS}	30 V
IRG4BC10K	IGBT	I_C	9,0 A	U_{CES}	600 V	U_{GE}	20 V

Tested elements are inserted in the test circuit through an additional adapter.

When inserting the elements, the following rules must be obeyed.

1. The adapter is permanently inserted into the right curve tracer socket and must not be removed.
2. Elements should be mounted so that their terminal arrangement is in accordance with the labelling on the adapter. Terminal arrangement of each transistor is shown in a figure in its datasheet.
3. Element's terminals must not be bent.
4. During measurements, irrespectively of the voltage applied in the circuit, the protective cover above the device mounting connectors must be closed.
5. Field effect transistors are very sensitive to electrostatic discharge that may cause gate breakdown and thus their permanent damage. Consequently, the following security measures must be taken:
   - elements presently not under test should be kept in the antistatic bag;
   - before grabbing an element it is necessary to remove any electrostatic charge that may be accumulated on one's body, by for example touching the mass of the oscilloscope;
   - an element should be held by its heat sink (the protruding part of the case) not by its terminals (pins).

Preliminary activities

1. Before the curve tracer is powered on:
   - ensure that in the right-hand side terminal sockets, a green adapter has been inserted with a socket for component mounting in the form of a blue triple screw terminal block;
   - if from under the security cover, wires are led out to the left with an external socket, put their plugs in the two lowest left-hand side sockets (labelled as E).
2. Prepare the curve tracer according to the guidelines found in the operating manual ("Setting up the curve tracer for work" box).

   While waiting for the CRT tube to warm up (the light spot to appear) one can proceed with step 3.

3. Verify if the camera settings are in accordance with those given in Section 4.2.b and make appropriate adjustments if necessary.
4. Calibrate the spot position on the curve tracer display:
   (a) press *Zero [C6]*;
   (b) if the spot is not located precisely in the lower left corner of the scale (not including the dashed lines), it is necessary to tune its position with light-grey knobs ↕ *Position [C2]* and ↔ *Position [C3]*, with the *Zero* button still pressed;
   (c) press *Cal [C6]* and check that the spot has moved by 10 divisions right and 10 divisions upwards.
5. Turn on the normal mode of characteristics tracing: *Mode [A5] = Norm.*

Warning! After finishing the laboratory session, independently of the number of measurements carried out, it is necessary to perform operations described in Section 5.4.

5.2. Characteristics of junction transistors

Measurement circuit set-up

Before proceeding it is absolutely obligatory to keep all the safety measures described in Section 5.1!

1. Find the discrete BJT transistor given in Table 1 (without any additional components attached). Using its datasheet, determine its terminal arrangement (C, B, E). Plug the transistor into the adapter's screw terminal, respecting the terminal labelling.
2. On the curve tracer, set:
   - common emitter configuration with base drive from the step generator: set the *terminal connection switch [D1]* to the *Step Gen* position within the *Emitter Grounded* range (exactly this setting, not any other),
   - the collector polarity with respect to the above selected common terminal (emitter) appropriate for the forward blocking and conduction states of an NPN transistor: *Polarity [A4]* = appropriate setting + (positive) or – (negative).
   - power limit of 2,2 W: *Max Peak Power [A1] = 2.2*,
   - current axis scale I_C (Y) of 10 mA: *Vertical Current/Div [C1] = Collector (not Emitter) 10 mA*,
   - voltage axis scale U_{CE} (X) of 0,5 V: *Horizontal Volts/Div [C7] = Collector (not Base) .5 V (not 5)*,
   - number of branches of the characteristic (not including the zero branch) to 1: *Number of Steps [B1] = 1*.

   Also ensure that the minimum, i.e., 0,05 μA, step generator current step ΔI_B is set: *Step/Offset Amplitude [B2] = .05 μA* (not any other unit, i.e., not mA nor V!)

Before proceeding with the next steps, connections and settings must be checked by the instructor!

3. Obtain a collector-emitter voltage of 5 V and supply the element under test:
   (a) turn the *Variable Collector Supply [A3]* knob until a section with a maximum voltage of 5 V is displayed on the screen;

   The *Variable Collector Supply* knob is scaled in percentage of the value set with the *Max Peak Volts [A1]* knob. It only allows coarse adjustment of the collector supply amplitude. The precise value must be set watching the screen.

   If at any time during exercise carrying out, curves observed on the screen are doubled in the form of loops (instead of single lines), this may be caused by an ambiguous *Display Invert [C5]* or *Zero [C6]* button position. When either button is slightly pushed and released, it should be put into a fully released position and bring the correct curve shapes back.

   The above situation may also have another cause, which cannot be eliminated completely. It is the presence of parasitic inductance which cause the operating point trajectory being different when the voltage across the device terminals is increased and when it is decreased.

   (b) turn on the step generator by pressing the *On* button in the *Step Family [B8]* group;
   (c) switch *Left-Off-Right [D2]* to *Right*.

   If instead of a single, horizontal section at the bottom of the screen (according to the remark above, a slight hysteresis is admissible) something else can be seen, immediately disconnect the supply of the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the instructor to check the measurement circuit once again.

Output characteristics of the discrete BJT

4. Display the first branch of the characteristics:
   (a) with the *Setup/Offset Amplitude [B2]* knob, increase the base current step ΔI_B until the first branch is raised above the X axis;

   If for the maximal step size ΔI_B = 200 mA the characteristics has not yet detached from the axis (a single horizontal line is still displayed at the bottom of the screen), disconnect the supply of the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the instructor to check the measurement circuit once again.

   (b) decrease the Y axis scale so that collector currents of up to 4 A can be optimally observed on the screen (i.e. maximally zoomed without the characteristics going beyond the screen; the word „can" meaning enabling observation, not that such currents should now be seen on the screen): *Vertical Current/Div [C1]* = appropriate *Collector* setting;
   (c) with the *Step/Offset Amplitude [B2]* knob set the base current to ΔI_B = 100 mA.
5. Display an entire family of output characteristics:
   (a) in order not to overheat the transistor, turn off the step generator: press *Step Family [B8] / Off*;
   (b) increase the maximum power dissipated in the transistor to 50 W: *Max Peak Power [A1] = 50*;
   (c) change the number of branches to 10 (not including the zero step): *Number of Steps [B1] = 10*;
   (d) press the *Single* button in the *Step Family [B8]* group; the screen should briefly display a set of 11 branches of the output characteristics for the transistor under test, $I_C = f(U_{CE}, I_B)$, the zero branch overlapping with the U_{CE} (X) axis as the *Zero* button has been pressed in the *Offset [B4]* group;

   If the *Single* button is pressed too frequently, this may cause transistor overheating as it is not well cooled. This button can be therefore used 1 to 3 times (one after another) and a break of at least 5 seconds must follow.

   (e) check (by pressing the *Step Family [B8] / Single* button) whether the highest branch crosses the 4 A current level in saturation mode (see Fig. 4) but does not exceed 4,5–5 A; increase or decrease the collector supply amplitude appropriately (*Variable Collector Supply [A3]* knob) if needed;

   if the above conditions cannot be reached, ask the teacher to check settings.
6. Record the characteristics image according to the procedure described below, which assures that the transistor—which is not cooled in any way—is not overheated due to excessive characteristics display time:
   (a) disconnect the power supply from the tested element by switching *Left-Off-Right [D2]* to *Off*;
   (b) turn on the step generator by pressing the *On* button in the *Step Family [B8]* group;
   (c) prepare to taking the picture turning on the self-timer;

   Pictures should be taken so that they capture not only the screen but also the settings displayed on the right-hand side of the display.

   Image quality is increased when the camera is placed closer to the screen.

   (d) press the camera shutter, without supplying the element under test now but watching the count-down on the camera screen, only ...
   (e) ... when the digit 1 is displayed on the camera screen, supply the device under test by switching *Left-Off-Right [D2]* to *Right* ...
   (f) ... and immediately after the shutter sound is heard, switch *Left-Off-Right* back to *Off*.
   (g) verify the quality of the image taken (see Section 4.2.a):

- the lines should not be too fuzzy—if needed, take the picture once again making sure that the camera is stable and waiting for the focus to be set correctly;
- make sure that the settings displayed on the right-hand side are visible—if not, take the picture once again;
- if the fine grid along central lines of the screen is not visible, adjust the graticule brightness with the *Graticule Illum* knob (upper left corner of the A group) and take the picture once again;
- check if the correct date has been imprinted in the bottom right corner of the picture, otherwise your results will be considered as cheated.

While carrying out the next step assure safety precautions as described in Section 5.1!

7. Place the element tested back in the antistatic bag.

Once the curve tracer has been powered on, it should not be turned off for the time switch-overs are made or components are replaced. However, one should always make sure that the *Left-Off-Right [D2]* switch is in its *Off* position.

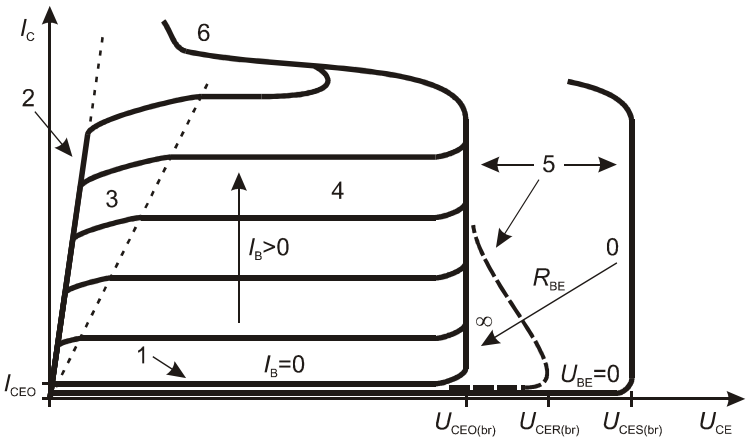


Fig. 4. Static output characteristic of the power BJT with operating modes marked: 1 – blocking, 2 – saturation, 3 – quasi-saturation, 4 – active, 5 – avalanche breakdown, 6 – thermal breakdown

Output characteristics of the BJT darlington

8. * On the curve tracer, set:
   - power limit of 2,2 W: *Max Peak Power [A1] = 2.2*,
   - minimal step generator current step ΔI_B: *Step/Offset Amplitude [B2] = .05 μA*,
   - voltage axis scale U_{CE} (X) of 1 V: *Horizontal Volts/Div [C7] = Collector 1 V*,
   - number of characteristic branches (not including the zero branch) to 1: *Number of Steps [B1] = 1.*
9. * While preserving safety precautions, find the BJT darlington to be investigated according to Table 1. Using its datasheet, determine the arrangement of its terminals (C, B, E). Plug the transistor into the adapter's screw terminal, respecting the terminal labelling.

Before proceeding to the next step, connections and settings must be checked by the instructor.

10. * Supply the element under test:
    (a) turn the *Variable Collector Supply [A3]* knob until a section with a maximum voltage of 10 V is displayed on the screen;

(b) turn on the step generator by pressing the *On* button in the *Step Family [B8]* group;

(c) switch *Left-Off-Right [D2]* to *Right*.

If instead of a single, horizontal section at the bottom of the screen (a slight hysteresis is admissible) something else can be seen, immediately disconnect the supply of the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the instructor to check the measurement circuit once again.

11. * Display a family of output characteristics:
    (a) with the *Step/Offset Amplitude [B2]*, set the base current step to $\Delta I_B = 5$ mA;
    (b) repeat step 5.
12. * Record the characteristics image by repeating step 6.
13. * Respecting safety precautions, place the element tested back in the antistatic bag.

5.3. Output characteristics of field-effect transistors

MOSFET

While carrying out the following step it is important to respect safety precautions as described in Section 5.1!

1. While preserving safety precautions, find the MOSFET given in Table 1. Using its datasheet, determine its terminal arrangement (D, G, S). Plug the transistor into the adapter's screw terminal, respecting the terminal labelling.
2. On the curve tracer, set:
   - power limit of 2,2 W: *Max Peak Power [A1] = 2.2*,
   - voltage axis scale U_{CE} (X) of 1 V: *Horizontal Volts/Div [C7] = Collector 1 V*,
   - drain polarity with respect to the previously selected common terminal (source) appropriate for the forward blocking and conduction states of an N-channel MOSFET (see Fig. 5 if in doubt): *Polarity [A4]* = appropriate setting + (positive) or – (negative).
3. Set up the step generator by setting:
   - the number of branches (excluding the zero one) to 1: *Number of Steps [B1] = 1*,

     Improper setting below may cause the transistor to be damaged!

   - the voltage step of the step generator ΔU_{GS} to 0,5 V: *Step/Offset Amplitude [B2] = .5 V* (not any other unit, i.e., not µA nor mA!),
   - the zero step level U_{GS0} to 3,5 V: the *Offset Mult [B3]* knob to a position corresponding to the $U_{GS0}/\Delta U_{GS}$ quotient,

     The *Offset Mult* knob is an accurate and delicate mechanical object. You should use it with caution and without exerting excessive force. If it does not move or is resistant, it should be unlocked using a small lever on its side.

     The current *Offset Mult* knob setting is read out as follows: the integer part above the black vertical mark, the tenth parts below. Since in the present exercise the *Number of Steps* setting is always an integer number, zero should be found below the mark after any adjustment is done.

   - *Offset Mult* knob activated: push *Aid* in the *Offset [B4]* group.

Before proceeding with the next steps, connections and settings must be checked by the teacher!

4. Display the first branch of the characteristics:
   (a) turn the *Variable Collector Supply [A3]* knob until a section with a maximum voltage of 10 V is displayed on the screen;
   (b) turn on the step generator by pressing the *On* button in the *Step Family [B8]* group;
   (c) switch *Left-Off-Right [D2]* to *Right*;

   If instead of one or more characteristic branches (the lowest ones can be very close one to another) something else can be seen, immediately disconnect the supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher to check the measurement set-up once again.

   (d) if only one branch of the characteristic (the zero one) can be seen on the screen, make the first branch appear: set the *Offset Mult [B3]* knob in a position corresponding to an integer number (i.e., with a decimal part of 0) higher than the present setting, such that two separate

branches, the zero and the first one, appear on the screen (they can be located very close one to another);

if the zero branch seen on the screen is not found on the X axis, bring it down to the axis level: set the *Offset Mult [B3]* knob to a position corresponding to an integer number (i.e., with a decimal part of 0) lower than the present setting, such that two separate branches, the zero and the first one, can be seen on the screen (they can be located very close one to another), with the zero one found on the X axis;

if the above conditions, i.e., an image of two characteristic branches with the zero one found on the X axis level, cannot be reached, ask the teacher to check settings.

5. Display an entire family of output characteristics:
   (a) in order not to overheat the transistor, turn off the step generator: press *Step Family [B8] / Off*;
   (b) increase the maximal power dissipated in the transistor to 50 W: *Max Peak Power [A1] = 50*;
   (c) using the *Number of Steps [B1]* knob increase the number of branches to 10;
   (d) press the *Single* button in the *Step Family [B8]* group; the screen should briefly display a set of 11 branches of the output characteristics for the transistor under test, $I_D = f(U_{DS}, U_{GS})$, the zero branch overlapping with the U_{DS} (X);

   For the MOSFET, within the range of drain currents visible, a few highest branches may overlap.

   (e) check (by pressing *Single [B8]*) whether the highest branch crosses the 4 A current level in linear mode (remember it is a MOSFET characteristic, see Fig. 5) but does not exceed 4,5–5 A; increase or decrease the collector supply amplitude appropriately (*Variable Collector Supply [A3]* knob) if needed;

   if the above conditions cannot be reached, ask the teacher to check settings;

   (f) imperatively write down the current *Offset Mult [B3]* knob setting.
6. Record the characteristics by repeating step 5.2/6.
7. Respecting safety precautions, place the element tested back in the antistatic bag.

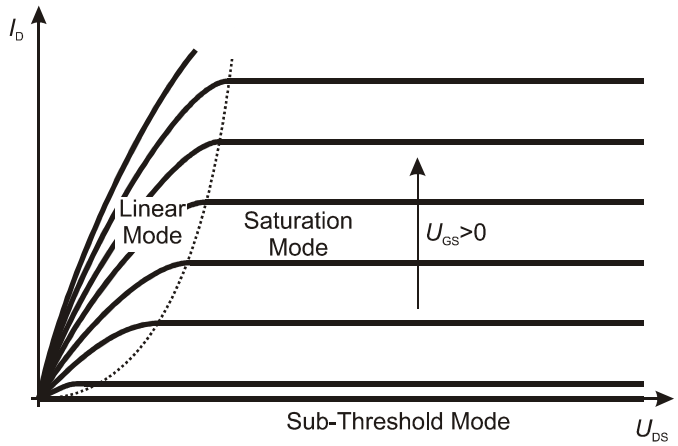


Fig. 5. Static forward output characteristic of an N-channel power MOSFET with operating modes tagged

IGBT

8. While preserving safety precautions, find the IGBT given in Table 1. Using its datasheet, determine its terminal arrangement (C, G, E). Plug the transistor into the adapter's screw terminal, respecting the terminal labelling.
9. On the curve tracer, set:
   - power limit of 2,2 W: *Max Peak Power [A1] = 2.2*,

- collector polarity with respect to the previously selected common terminal (emitter) appropriate for the forward blocking and conduction states of an N-channel IGBT (see Fig. 6 if in doubt): *Polarity [A4]* = appropriate setting + (positive) or – (negative).

10. Set up the step generator by setting:
    - the number of branches (excluding the zero one) to 1: *Number of Steps [B1] = 1*,
    - the voltage step of the step generator ΔU_{GE} to 1 V: *Step/Offset Amplitude [B2] = 1 V* (not any other unit),
    - the zero step level U_{GE0} to 6,0 V: the *Offset Mult [B3]* knob to a position corresponding to the $U_{GE0}/\Delta U_{GE}$ quotient.

Before proceeding with the next steps, connections and settings must be checked by the instructor.

11. Display the entire family of curves by repeating steps 4 and 5 entirely.
12. Record the characteristics image by repeating step 5.2/6.
13. Respecting safety precautions, place the element tested back in the antistatic bag.

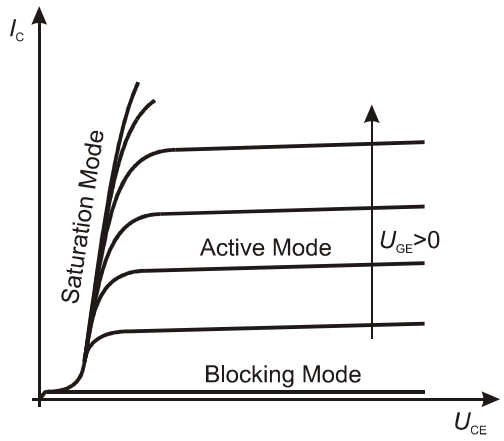


Fig. 6. Static forward output characteristic of an N-channel IGBT with operating modes labelled

5.4. Measurement termination

1. Ensure that the supply is disconnected from the device under test: *Left-Off-Right [D2]* is set to *Off*.
2. Bring curve traces settings back to safe ones:
   - zero collector voltage: turn *Variable Collector Supply [A3]* maximally counterclockwise,
   - power limit of 0.1 W: *Max Peak Power [A1]* = 0.1,
   - minimum current step ΔI_B: *Step/Offset Amplitude [B2]* = *.05 μA*,
   - step generator turned off: push *Step Family [B8]* / *Off*,
   - Y axis scale of 10 mA/div: *Vertical Current/Div [C1]* = *Collector 1 mA*,
   - *Offset Mult* knob de-activated: push *Offset [B4]* / *Zero*.
3. Turn off the curve tracer: switch *Power [A2]* to *Off*.
4. Copy the pictures taken to the team's account on the PC and erase them from the camera (see Section 4.2.c).

D

Results

6. Result Elaboration and Analysis

6.1. Input and output quantity values

1. In the static output characteristics of tested devices:
   (a) for each of the 3 devices (* excluding the darlington) mark and label the different regions of operation (see Figs. 4, 5 and 6);
   (b) for all 3 (* 4, darlington included) devices, label the different branches of the family of characteristics with corresponding drive current or voltage (as appropriate) values; use the formulae (4.3) and (4.2) and the following data:
      - the indication in the *PER STEP* field in the captured images (the *Step/Offset Amplitude* setting, which is the step of the step generator, ΔI_B (or ΔU_{GS} and ΔU_{GE} as appropriate),
      - the setting of the *Offset Mult* knob written down (steps 5.3/5(f) and 11) which enables calculating the step generator zero step level I_{B0} (thus, U_{GS0} or U_{GE0} as appropriate),
      - knowledge that for the BJTs, the *Offset/Zero* button was pressed.

      Remember that the lowest branch corresponds to $n = 0$ (not 1).

2. For the discrete BJT (* and for the Darlington), for 4 values of the load current $I_o = I_C$ = 0.5 A, 1 A, 2 A, 4 A:
   (a) in the recorded characteristics, mark the point corresponding to the operation in the saturation region;

      Draw—on paper, computer or in imagination—a straight line parallel to the voltage axis, lying at the level of the given load current I_o. Then, moving left along this line, reach such a U_{CE} voltage value that the crossing point of this line with the characteristics branch is located in the full saturation region (not the quasi-saturation one).

   (b) read out and write down the 3 coordinates of this point (see correct reading example shown in Fig. 7):
      - the on-state main voltage $U_{on} = U_{CE} = U_{CE(sat)}$ (with an accuracy of 0.1 div),

- the main current $I_o = I_C$ (which should be one of the values given above),
- the input current $I_{in} = I_B$ (with an accuracy equal to the step of the step generator, using the labels written in the image);

(c) from the data sheet, read the input voltage value $U_{in} = U_{BE}$ corresponding to the saturation region at the given value of the output current I_o [the $U_{BE(sat)} = f(I_C)$ characteristic].

Due to the short duration of measurements made, it can be assumed that transistors were not heating up, hence the temperature of each semiconductor structure was equal to the room temperature. Readouts of all temperature-dependent parameters should therefore be made for the junction temperature T_j = 25 °C.

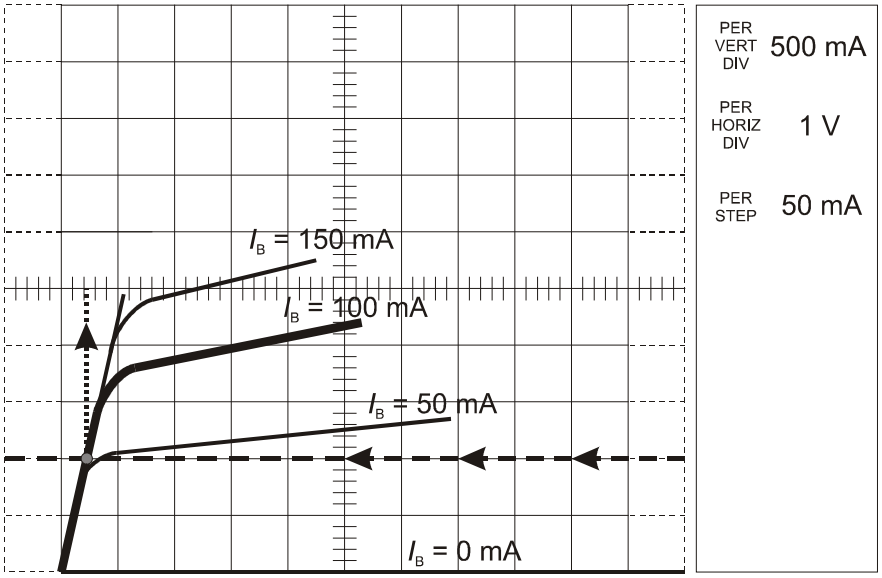


Fig. 7. An example of localisation of an operating point of a BJT that lies in the saturation region, for the load current I_o = 1 A (the remaining coordinates are $U_{on} \approx 0.4$ V and $I_{in} \approx 100$ mA). Curves in the image are idealised and do not have any quantitative connection with those obtained in the present exercise.

3. For the MOSFET and the IGBT, for 4 values of the load current $I_o = I_D$ or I_C accordingly = 0.5 A, 1 A, 2 A, 4 A:

(a) in the recorded characteristics, mark the point corresponding to the operation in the linear (MOSFET) or saturation (IGBT) region with a low on-state main voltage drop;

(b) read out and write down the 3 coordinates of this point (see correct reading example shown in Fig. 8):

- the on-state main voltage $U_{on} = U_{DS}$ or $U_{on} = U_{CE} = U_{CE(sat)}$ accordingly (with an accuracy of 0.1 div),
- the main current $I_o = I_D$ or $I_o = I_C$ (which should be one of the values given above),
- the input voltage $U_{in} = U_{GS}$ lub $U_{in} = U_{GE}$ accordingly (with an accuracy equal to the step of the step generator, using the labels written in the image);

The definition of a '*low* voltage drop' is obviously not precise. However, characteristics branches exhibit a tendency to become closer to each other as the drive voltage increases, and finally they create a single thick line on the screen. It should be assumed that the voltage is 'low' when a given branch is indistinguishable from the leftmost one (following the horizontal line corresponding to the given load current, as presented in Fig. 8).

(c) from the gate charge characteristic given in the data sheet, read out the charge flowing in the input circuit during transistor switching $Q_{in} = Q_{G(tot)}$ corresponding to the input voltage determined in sub-step (b) (see Section 3.2.d).

If the gate charge characteristic is available for several values of the main voltage, choose the branch corresponding to the value closest to the transistor's rated voltage. Neglect the dependence of this characteristic on the main current, however, conform to guidelines given in Section 3.2.d.

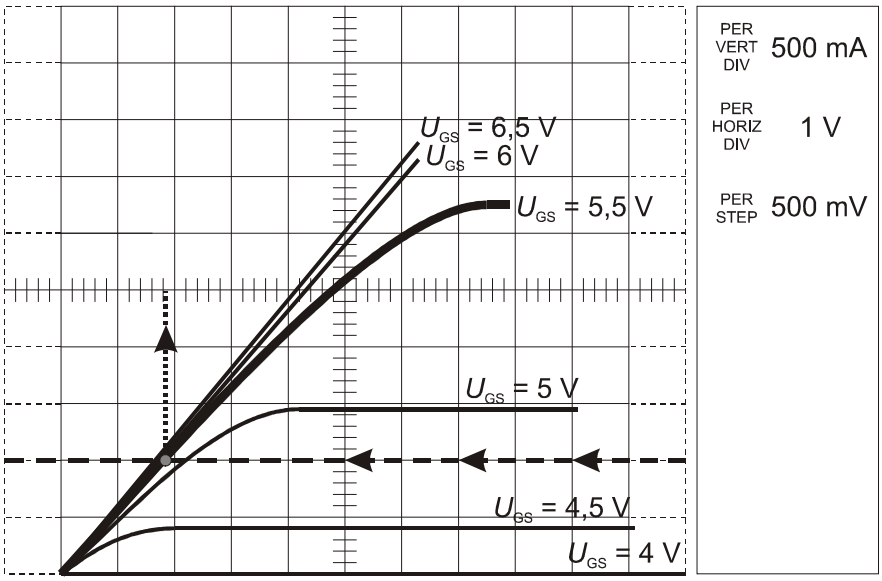


Fig. 8. An example of localisation of an operating point of a MOSFET that lies in the linear region and where the on-state main voltage drop is low, for the load current I_o = 1 A (the remaining coordinates are $U_{on} \approx 1{,}8$ V and $U_{GS(min)} \approx 5{,}5$ V). Curves in the image are idealised and do not have any quantitative connection with those obtained in the present exercise.

4. Collect the numerical results in a separate table for each of the 3 (*4) transistors (or in one common table but , however it will have to be split in the report).
5. Based on the results obtained in steps 2—3, for each of the 3 (*4) transistors, calculate the on-state resistance

$$R_{on}(I_o) = \frac{U_{on}(I_o)}{I_o} \tag{6.1}$$

6. Based on the results from steps 2—3, for each of the 3 (*4) transistors and for each of the 4 load current values, calculate the static power loss in the main circuit P_{main} (see Section 3.1.d). Add results to the tables.

   This procedure requires definite operating conditions to be assumed. They have to be identical and reasonable for all the transistors so as reliable comparisons could be made. For the purpose of this exercise, the simplest case of switching operation with a duty cycle $D = 0.5$ should be assumed.
7. Based on the results from steps 2—3, for each of the 3 (*4) transistors and for each of the 4 load current values, calculate the drive power P_{drv} (see Section 3.2). Add results to the tables.

   In order for the results to be coherent, the previous assumption of $D = 0.5$ should be maintained. To calculate power for the charge-controlled devices, it is necessary to additionally assume a definite switching frequency f_s. The value of 10 kHz should be assumed, which is an approximate application borderline between bipolar junction transistors and unipolar field-effect transistors.

6.2. Static properties analysis

1. Analyse the on-state voltage drop U_{on} (a 'decent' on-state, which we have considered to be full saturation or linear with a low voltage drop):
   (a) Based on result tables, plot the on-state voltage drop U_{on} as function of the main current I_o [all 3 (*4) devices in a single graph], however, exchanging the axes to obtain a coordinate system as for the output characteristic (voltage on the x-axis and current on the y-axis). The coordinate system should begin at the (0, 0) point.

   The last statement of the above sub-step does not mean that a (0, 0) point should be added to the measurement data since such a point was not read out, nor does it mean that approximated characteristics are to be drawn in this range as this would require a much larger number of points to be read out.

   (b) Based on result tables, plot the on-state resistance R_{on} as function of the main current I_o [all 3 (*4) characteristics in a single graph]. To ease determination of the character of the relationship, use logarithmic scale for <u>both</u> axes.
   (c) Determine the character of the observed relationships. Can bipolar and unipolar devices (see Manual 0, Ref. H) be discerned considering this character (i.e., based on the rate of change with the current, not the values as such)? Specifically list devices that belong to either group. Point out what specifically the similarity between devices within either group consists in.
   (d) Explain the observation from sub-step (c) using your knowledge on current conduction mechanisms (refer to the results obtained in Exercise 1). Point out devices which exhibit conductivity modulation of the lightly doped layer (justify).
   (e) What do the differences between the following transistors consist in:
      - different bipolar ones?
      - * discrete and Darlington BJT?

      Only consider parameters investigated in this step. Analyse both the values (high / low) and their variability as function of current (rising / falling; strongly / weakly). Specifically list devices that belong to either group.
   (f) Can any features be pointed out that are common to all the voltage-charge-controlled transistors? (The analysis guidelines from the previous sub-step still apply.)
2. Analyse the static power loss in the main circuit P_{main}:
   (a) Based on result tables, plot the static power loss in the main circuit P_{main} as function of the main current I_o [all 3 (*4) devices in a single graph]. Due to the broad range of power values (more than one order of magnitude), plot the graph <u>both</u> using linear and logarithmic scales (always the same for both axes).
   (b) Determine the character of the observed relationships. Relate your observation to results obtained in step 1, referring to algebraic formula coupling the power and the voltage drop.

   Consider the properties of the logarithmic plot with regard to the character of a relationship (especially linear law and power laws; refer back to Exercise 1).

   (c) Based on results obtained, complement the transistor comparison from step 1(c), (e) and (f). Consider the <u>entire range</u> of main current for which measurement results are available and, in addition, based on the logarithmic plot, <u>make predictions</u> for lower and higher current values.
   (d) Draw conclusions on the application value of transistors of the different types considering the static power loss in the main circuit (<u>ignore</u> any other criteria). Take into account the <u>dependence on the load</u> (i.e., main) <u>current</u> which (current) would be forced by an application.

3. Analyse the drive power P_{drv}:
   (a) Based on result tables, plot the drive power P_{main} as function of the main current I_o using logarithmic scale for both axes [all 3 (*4) devices in a single graph].
   (b) Can current-controlled and charge-voltage-controlled devices (see Manual 0, Ref. H) be discerned considering both value of drive power and its rate of change with current? Specifically list devices that belong to either group. Point out what specifically the similarity between devices within either group consists in.
   (c) Explain observations from sub-step (b) using your knowledge about transistor drive mechanisms (current, see Ref. A; and voltage-charge, see Manual 3^A, Refs. A and B; in general, see Manual 0, Ref. H).
   (d) What do the differences between the following transistors consist in:
      - different voltage-charge-controlled devices?
      - * discrete and Darlington BJT?

      Apply all the guidelines from sub-step 1(e) in your analysis.
   (e) Can any features be pointed out that are common to all the bipolar transistors? (Apply guidelines as above.)
4. * Based on information, formulae and circuit schematic provided in Ref. B, explain the differences observed between the discrete and the Darlington BJT.
5. Formulate final conclusions concerning the application value of the different transistors for various possible applications:
   - requiring low drive power,
   - requiring low main circuit static power loss,
   - requiring both low drive and low main circuit static power loss.

   Consider only the static properties investigated in the present exercise, including the dependence on load current.
6. Based on results from steps 1—5 and from part B of this exercise regarding price relationships, point out reasons for applying BJTs:
   (a) discrete ones,
   (b) * darlingtons.

E

Information

7. Expected Report Contents

- Recorded characteristics labelled according to step 6.1/1 and with points marked according to step 6.1/2–3
  (i.e., photographs of output characteristics of transistors of different types, where regions of operations have been labelled and points have been marked for which coordinates were read out and put in the tables)
- Tables containing values read out in steps 6.1/2–3 and calculated in steps 6.1/5–7 together with formulae used, each placed below the curve tracer image for the respective transistor
  (i.e., main current, on-state main circuit voltage drop, input current or voltage, on-state resistance, main circuit static power loss, drive power and parameters read out from a data sheet necessary for its calculation)
- Plot of the on-state voltage as function of load current in the form of the output characteristics, plot of on-state resistance as function of load current, and their analysis, according to step 6.2/1
  (i.e., $U_{on} = f(I_o)$ plot but with U_{on} put on the X axis, using linear scale, and $R_{on} = f(I_o)$ using logarithmic scale, all transistors in one graph)
- Plots of main circuit static power loss as function of load current and their analysis, according to step 6.2/2
  (i.e., $P_{main} = f(I_o)$ plot using linear and logarithmic scales, all transistors in either graph)
- Plot of drive power as function of load current and its analysis, according to step 6.2/3
  (i.e., $P_{drv} = f(I_o)$ plot using logarithmic scale, all transistors in one graph)
- * Explanation of differences between BJTs, according to step 6.2/4
- Final conclusion with both power and drive circuit properties considered, with an additional analysis of the BJT, according to steps 6.2/5–6

8. Required Knowledge

8.1. Prerequisites

- Main circuit and drive circuit terminals, static output characteristics and regions of operation for power BJT, MOSFET and IGBT
  (see Ref. A; Manual 3^{A}, Ref. A; Manual 4^{A}; figures in Chapters 5.2 and 5.3)
- General operating principle of the curve tracer used in this exercise for the BJT output characteristic measurement case: collector supply (maximum voltage), gate generator (generator step, zeroth branch current)
  (see Section 4.1)

8.2. Test scope

1. High-voltage BJT: terminals, semiconductor structure cross-section, static output characteristic; operating regions—general picture of physical phenomena (especially, junction biasing and excess free carrier extension), location in the output characteristic); the difference in static and dynamic parameters between saturation and quasi-saturation
   (see Ref. A, Manual 0, Ref. H, 3.1.2)
2. Current gain (common-emitter) of the BJT: definition (formula), typical values for power transistors, dependence on collector current (plot, physical origins)
   (see Ref. A)
3. Darlington BJT: circuit schematic, current gain (as function of the two component transistor gains, typical values), voltage drop, main circuit power loss and drive power (in relation to the discrete BJT), advantages and drawbacks
   (see Ref. B, report)
4. Power transistor classification based on the drive (control) mechanism criterion and the conduction mechanism criterion—as applied to the devices investigated
   (see Manual 0, Ref. H, report)
5. Forward output characteristics, main circuit power loss and drive power as function of main current for the transistors of 3 different types (discrete BJT, MOSFET, IGBT) combined in a single plot (linear or logarithmic scale as in the report); connection to physical drive and conduction mechanisms
   (see report, Manual 0, Ref. H)
6. Advantages and drawbacks of the different 3 transistors (discrete BJT, MOSFET, IGBT) considered as power electronic switches, with regard to the power (main) circuit and with regard to the drive circuit; resulting potential application areas (including the dependence on load current); reasons for BJT application
   (see report)

9. References

[1] Benda V., Gowar J., Grant D. A.: *Power Semiconductor Devices: Theory and Applications.* Wiley, 1999. ISBN 0-471-97644-X.