⊞ Lattice®
Semiconductor Corporation

2000E, 2000VE and 2000VL Family Architectural Description

Introduction

The basic unit of logic for the ispLSI 2000E, 2000VE and 2000VL device families is the Generic Logic Block (GLB). Figure 1 illustrates the ispLSI 2128E with its 32 GLBs labelled A0, A1 .. D7. There are a total of eight GLBs in the ispLSI 2032E device, increasing to 32 GLBs in the ispLSI 2128E device. Each GLB has 18 inputs, a programmable AND/OR/XOR array and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the Global Routing Pool (GRP) and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

The devices also have 32 to 192 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output, bi-directional I/O pin with 3-state control or open-drain output. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two ORPs and two dedicated inputs are connected together to make a Megablock (16 I/O cells and one ORP in half-I/O versions). The outputs of the eight GLBs are connected to two sets of 16 universal I/O cells by the two ORPs. Each Megablock generates a common Product Term Output Enable (OE) signal which is available, along with the Global OE signal(s), to all I/O cells in the device. The ispLSI 2128E device, shown in Figure 1, contains four Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the devices are selected using Dedicated Clock Input pins or Product Term Clocks. The dedicated clock pins, Y0, Y1 and Y2, drive the global clocks, CLK 0, CLK1 and CLK 2.

Figure 1. ispLSI 2128E Block Diagram
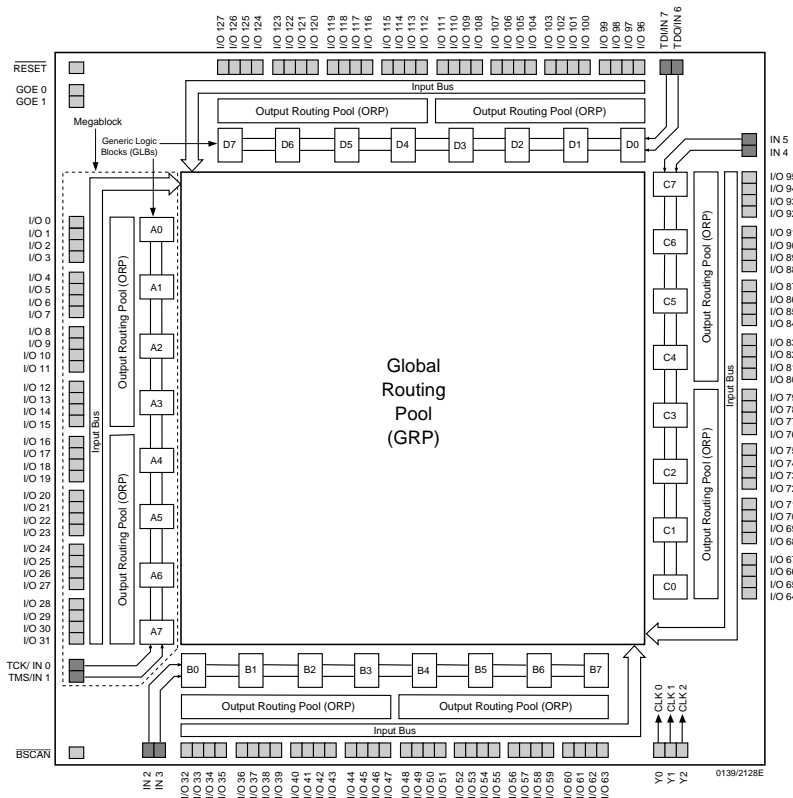
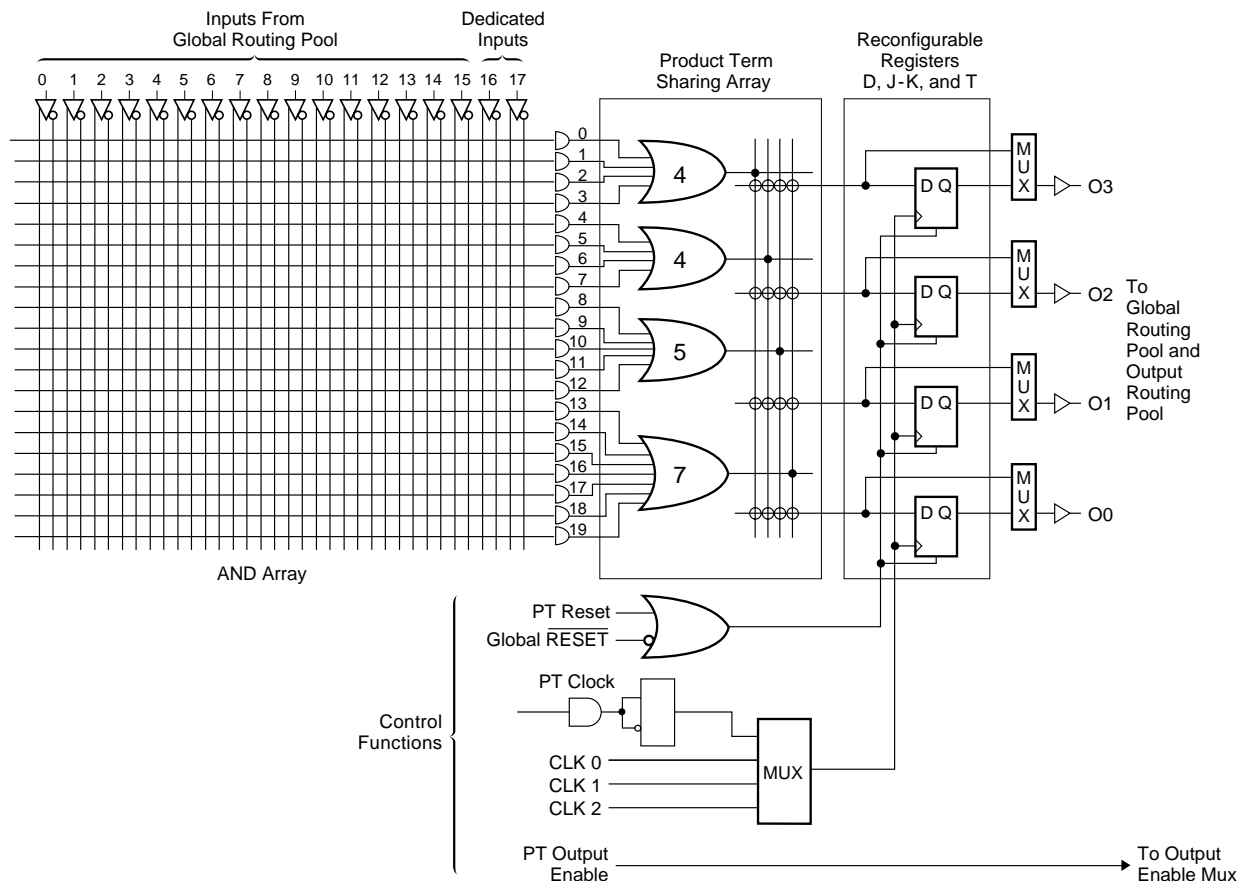# 2000E, 2000VE and 2000VL Family Architectural Description

Generic Logic Block

The Generic Logic Block (GLB) is the standard logic block of the Lattice High-Density ispLSI devices. A GLB has 18 inputs, four outputs and the logic necessary to implement most standard logic functions. The internal logic of the GLB is divided into four separate sections: the AND Array, the Product Term Sharing Array (PTSA), the Reconfigurable Registers, and the Control Functions (Figure 2). The AND array consists of 20 product terms which can produce the logical sum of any of the 18 GLB inputs. Sixteen of the inputs come from the Global Routing Pool, and are either feedback signals from any of the GLBs or inputs from the external I/O cells. The two remaining inputs come directly from two dedicated input pins. These signals are available to the product terms in both the logical true and the complemented forms which makes boolean logic reduction more efficient.

The PTSA takes the 20 product terms and routes them to the four GLB outputs. There are four OR gates, with four, four, five and seven product terms each (Figure 2).

The output of any of these OR gates can be routed to any of the four GLB outputs, and if more product terms are needed, the PTSA can combine them as necessary. In addition, the PTSA can share product terms similar to a PLA device. If the user's main concern is speed, the PTSA can use a bypass circuit which provides four product terms to each output, to increase the performance of the cell (Figure 3). This can be done to any or all of the four outputs from the GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an XOR gate on the input. The XOR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K or T-type flip-flop (Figure 4). This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Access to the XORs is not available when the four product term bypass is used.
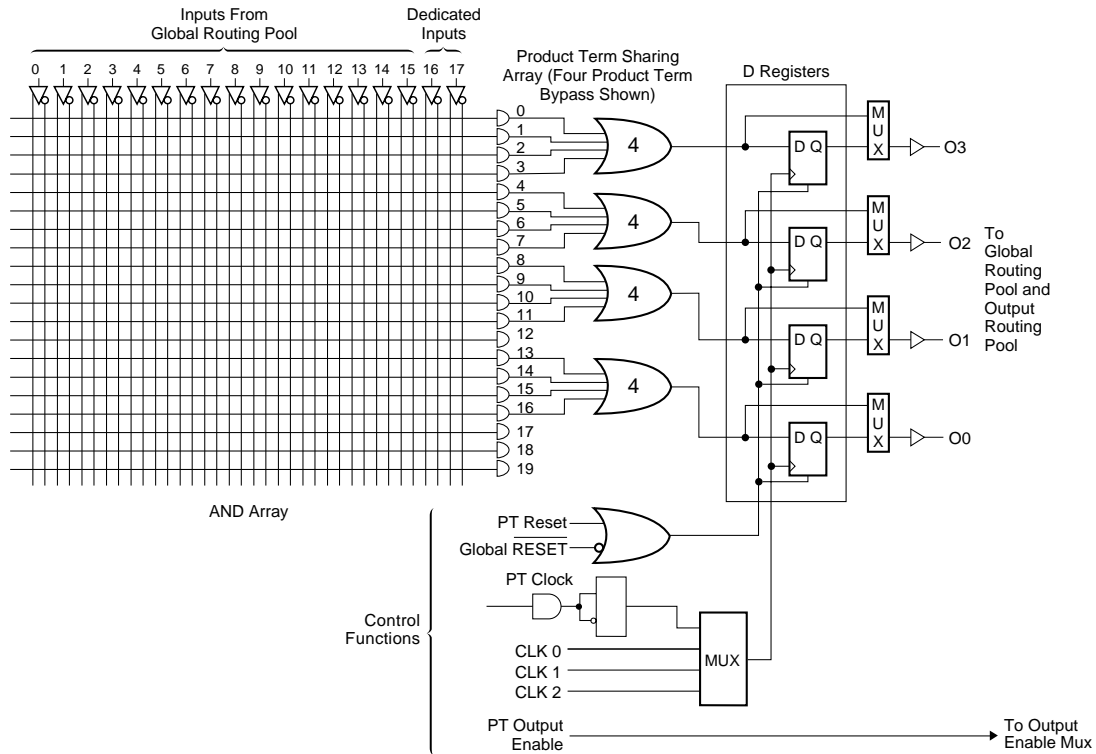
Figure 2. GLB: Product Term Sharing Array Example
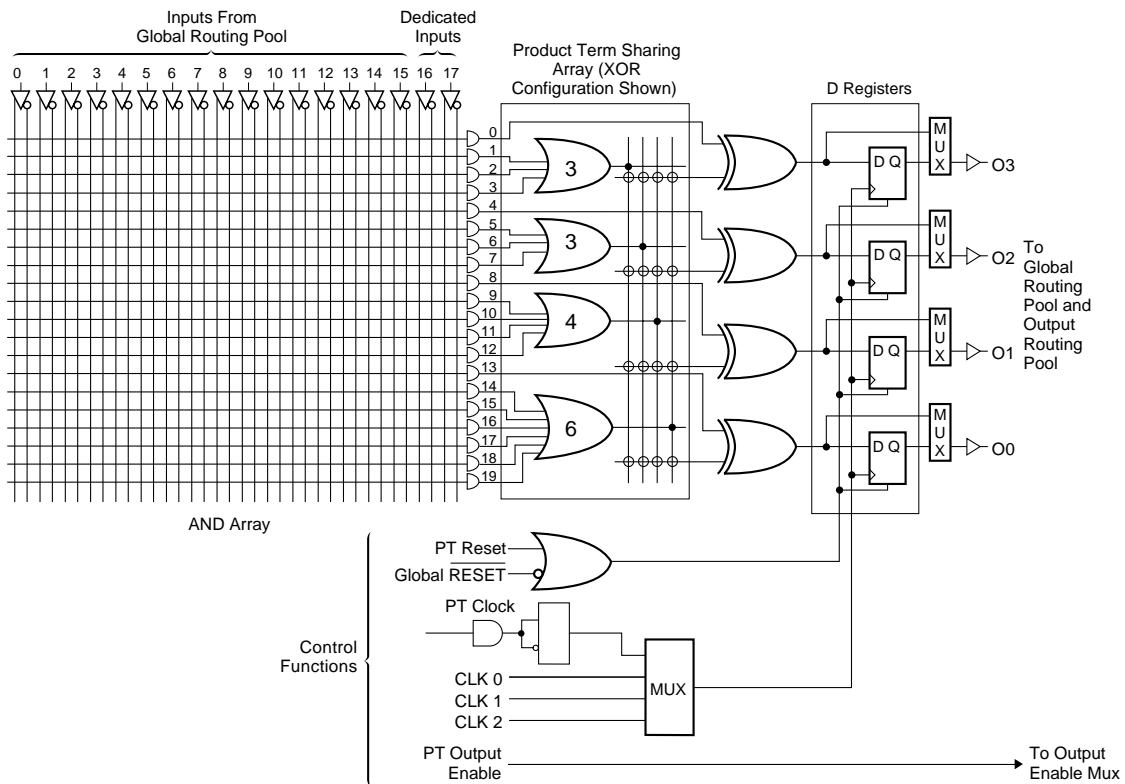

0130A/2000

2

Figure 3. GLB: Four Product Term Bypass Example

0131A/2000

Figure 4. GLB: XOR Gate Example

0132A/2000

Generic Logic Block (continued)

The PTSA is flexible enough to allow these features to be used in virtually any combination the user desires. In the GLB shown in Figure 5, Output Three (O3) is configured using the XOR gate while Output Two (O2) is configured using the four Product Term Bypass. Output One (O1) uses one of the inputs from the five Product Term OR gate while Output Zero (O0) combines the remaining four product terms with all of the product terms from the seven Product Term OR gate for a total of eleven (7+4).

Various signals which control the operation of the GLB outputs are driven from the Control Functions. The clock for the registers can come from any of three sources developed in the Clock Distribution Network (see the Clock Distribution section) or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin or from a product term within the block. The global reset pin is always connected and is logically "ORed" with the PT reset (if used). An active reset signal always sets the Q of the registers to a logic 0 state. The Output Enable for the I/O cells associated with the GLB comes from a product term within the block, or from one of the global OE pins. Use of a product term for a control function makes that product term unavailable for use as a logic term. Refer to the Product Term Sharing Matrix (Table 2) to determine which logic functions are affected.

There are many additional features in a GLB which allow implementation of logic intensive functions. These features are accessible using the hard macros from the software and require no intervention on the part of the user.

Figure 5. GLB: Mixed Mode Configuration Example
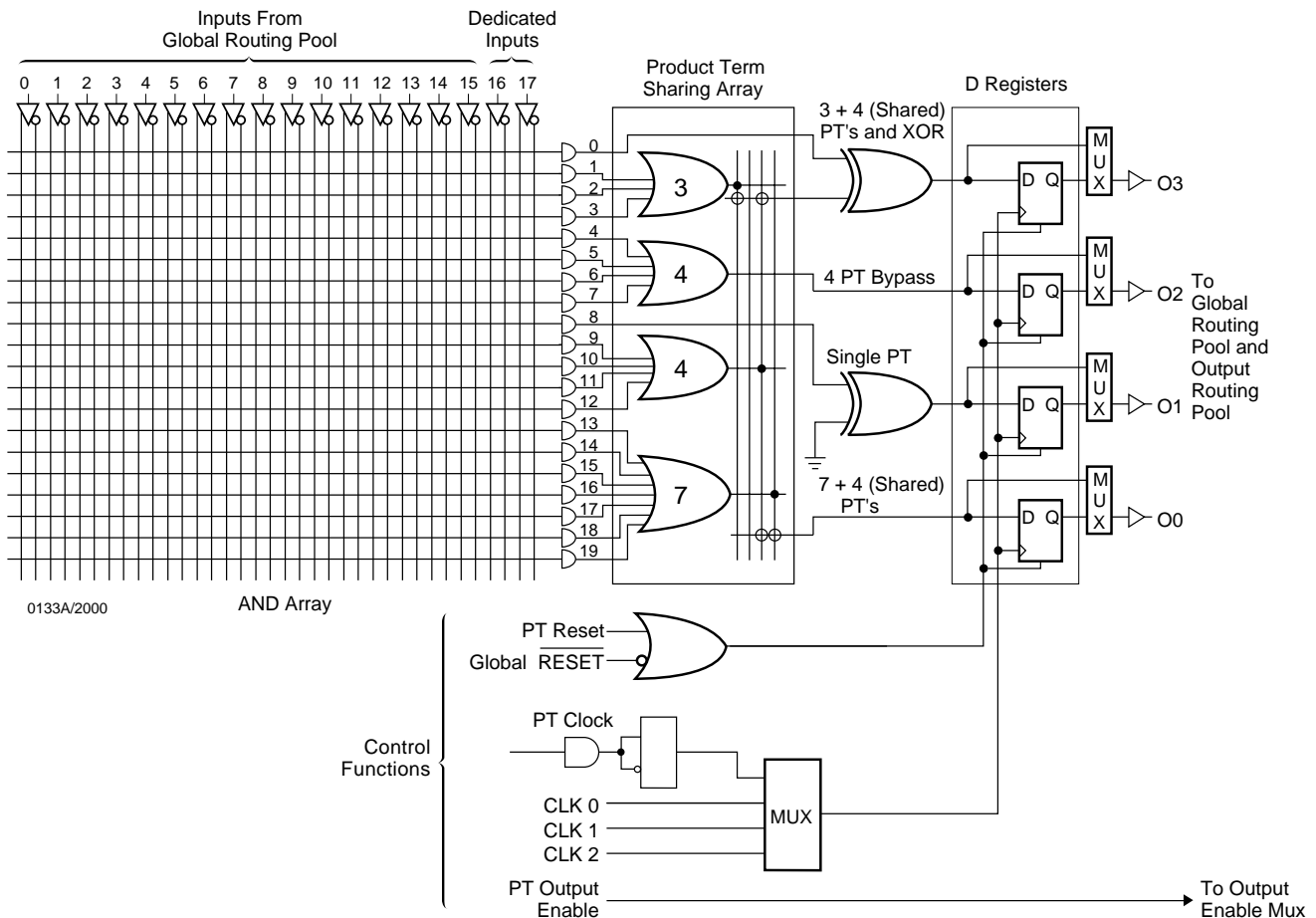
Product Term Sharing Matrix

This matrix shows how each of the product terms are used in the various modes. As an example, Product Term 12 can be used as an input to the five input OR gate in the standard configuration. This OR gate under standard configuration can be routed to any of the four GLB outputs. Product Term 12 is not used in the four product term bypass mode. When GLB output one is used in the XOR mode Product Term 12 becomes one of the inputs to the four input OR Gate. If Product Term 12 is not used in the logic, then it is available for use as either the Asynchronous Clock signal or the GLB Reset signal.

Table 2. Product Term Sharing Matrix

Product Term #	Standard Configuration Output Number				Four Product Term Bypass Output Number				Single Product Term Output Number				XOR Function Output Number								Alternate Function
	3	2	1	0	3	2	1	0	3	2	1	0	3	3	2	2	1	1	0	0	
0	■	■	■	■	■				■				■								
1	■	■	■	■	■									■							
2	■	■	■	■	■									■							
3	■	■	■	■	■									■							
4	■	■	■	■		■				■					■						
5	■	■	■	■		■										■					
6	■	■	■	■		■										■					
7	■	■	■	■		■										■					
8	■	■	■	■			■				■						■				
9	■	■	■	■			■											■			
10	■	■	■	■			■											■			
11	■	■	■	■			■											■			
12	■	■	■	■														■			■CLK/Reset
13	■	■	■	■				■				■							■		
14	■	■	■	■				■												■	
15	■	■	■	■				■												■	
16	■	■	■	■				■												■	
17	■	■	■	■																■	
18	■	■	■	■																■	
19	■	■	■	■																■	■OE/Reset

0215/2000

Megablock

The ispLSI 2000E, 2000VE and 2000VL Family Megablock consists of eight GLBs, two ORPs, 32 I/O cells, (one ORP and 16 I/O cells in half-I/O versions, two dedicated inputs and a common product term OE. The various members of the ispLSI 2000 Families combine from one to six Megablocks on a single device.

The eight GLBs within the Megablock share two dedicated input pins. These dedicated input pins are not available to GLBs in any other Megablock. These pins are dedicated (non-registered) inputs only and are automatically assigned by software. The product term OE is generated within the Megablock and is common to all 32 of the I/O cells in the Megablock. This OE signal can be generated using PT19 in any of the eight GLBs within the Megablock. There are also one or two dedicated OE inputs which can control from one to all of the I/O cells on the device (see the section on Output Enable Control for further details).

Table 3. Device Resources

ispLSI Devices	Megablocks	GLBs	I/Os	Dedicated Inputs	Global OE Pins
2032E, 2032VE, 2032VL	1	8	32	2	1
2064E, 2064VE, 2064VL	2	16	64/32	4	2
2096E, 2096VE, 2096VL	3	24	96	6	2
2128E, 2128VE, 2128VL	4	32	128/64	8	2
2192VE, 2192VL	6	48	96	9 or 12	2

Figure 6a. Megablock Block Diagram, Devices With All I/Os Used

0028C/2000
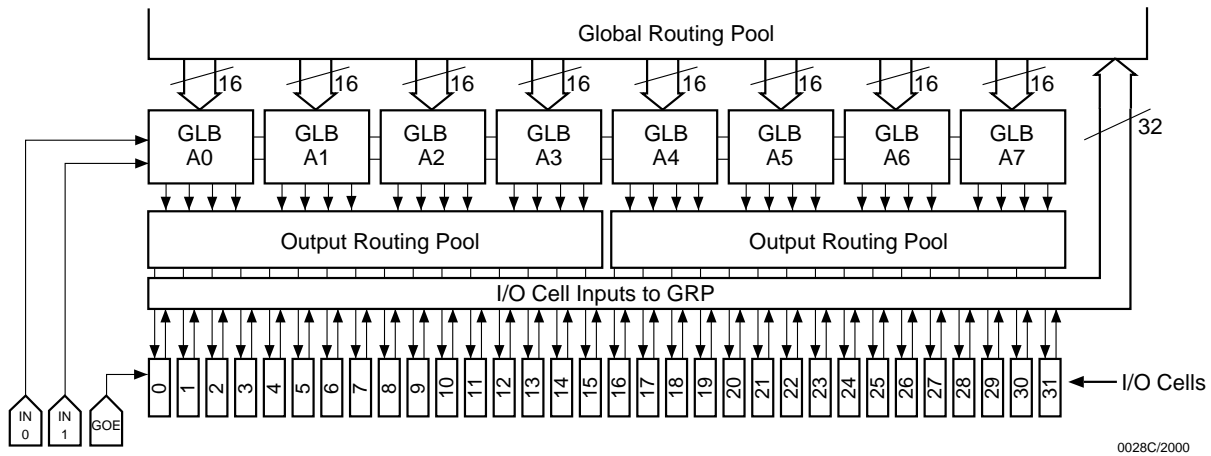
Figure 6b. Megablock Block Diagram, Devices With Half I/Os Used
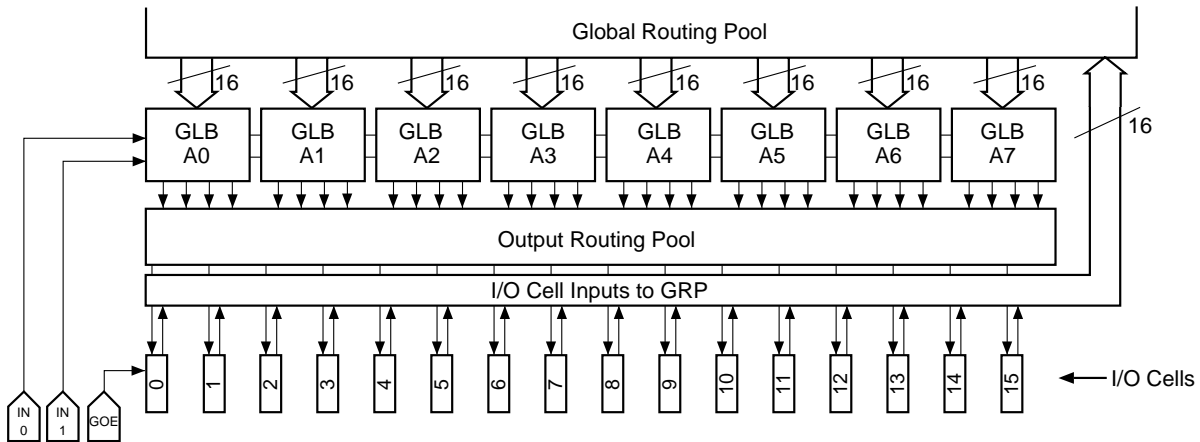
Input Routing

Signal inputs are handled in two ways within the device. First, each I/O cell within the device has its input routed directly to the GRP. This gives every GLB within the device access to each I/O cell input. Second, each Megablock has two dedicated inputs which are directly routed to the eight GLBs within the Megablock. Both input paths are shown in Figures 6a and 6b.

Output Routing Pool (ORP)

For the ispLSI 2000E, 2000VE and 2000VL devices (full I/O versions), each megablock contains two ORPs to increase output routability. A set of four GLBs is associated with one of the two ORPs within the megablock. The 16 outputs of the four GLBs within a megablock can feed up to 4 of the 16 associated I/O cells. The 32 GLB outputs of a megablock in these devices can feed 32 I/O cells. As illustrated in Figure 7, there is an equal number of I/O pins and logic macrocells. Each GLB output has ORP bypass capability so more designs can have critical output signals, as shown in Figure 8.

Some of ispLSI 2000VE and 2000VL devices are available in half I/O (one I/O pin per two GLB outputs). In these devices, each megablock contains the same structure as the 1000/E Family where only one ORP that feeds 16 I/O pins (Figures 9 and 10).

Figure 7. ispLSI 2000E, 2000VE and 2000VL Family Output Routing Pool (Full I/O Versions)
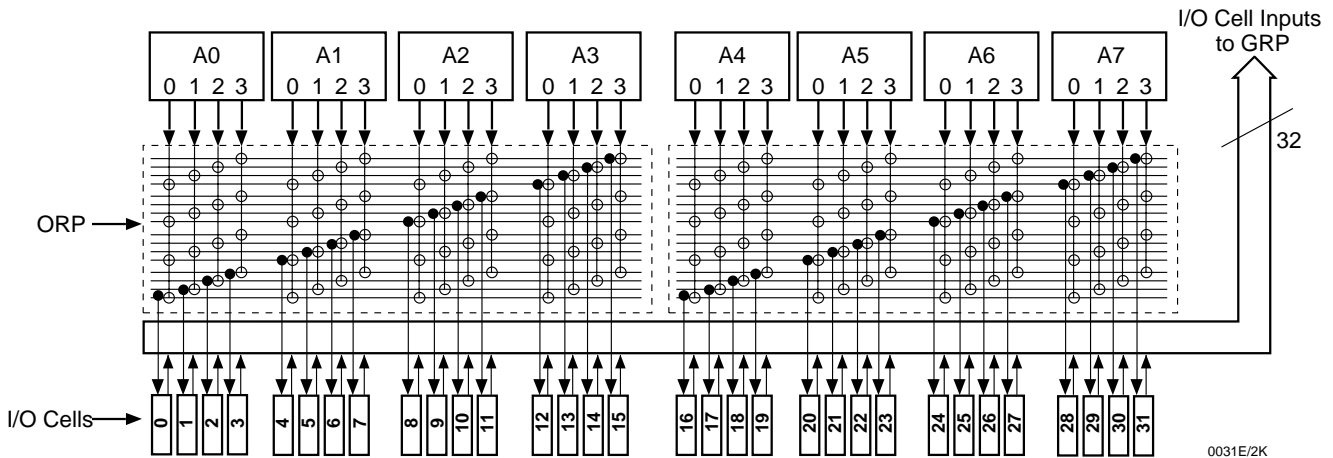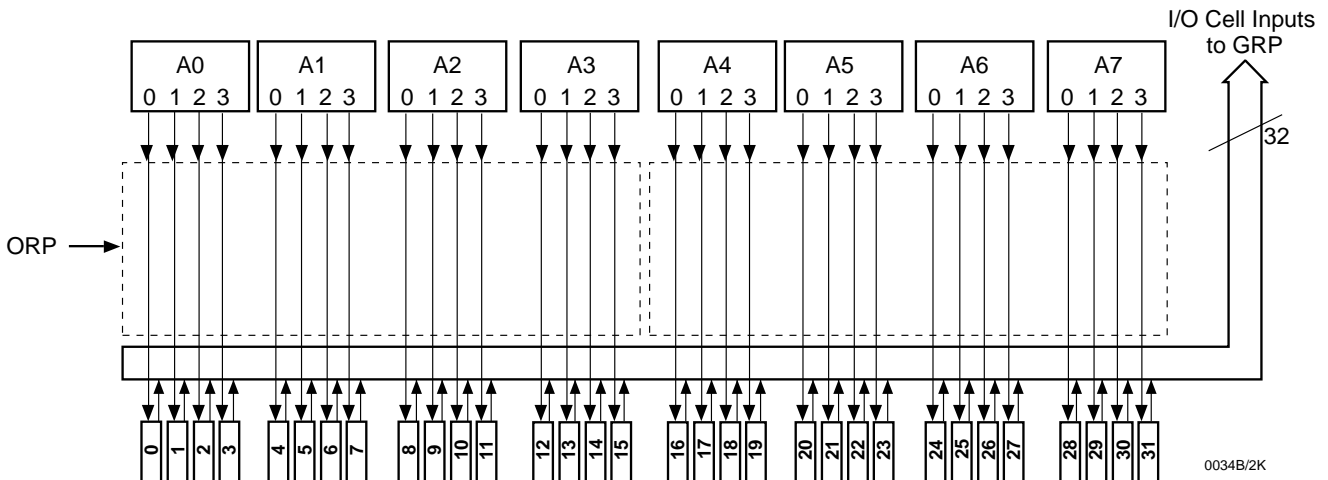

Figure 8. ispLSI 2000E, 2000VE and 2000VL Family Output Routing Pool Showing Bypass (Full I/O Version)

7

Figure 9. ispLSI 2000E, 2000VE and 2000VL Family Output Routing Pool (Half I/O Versions)
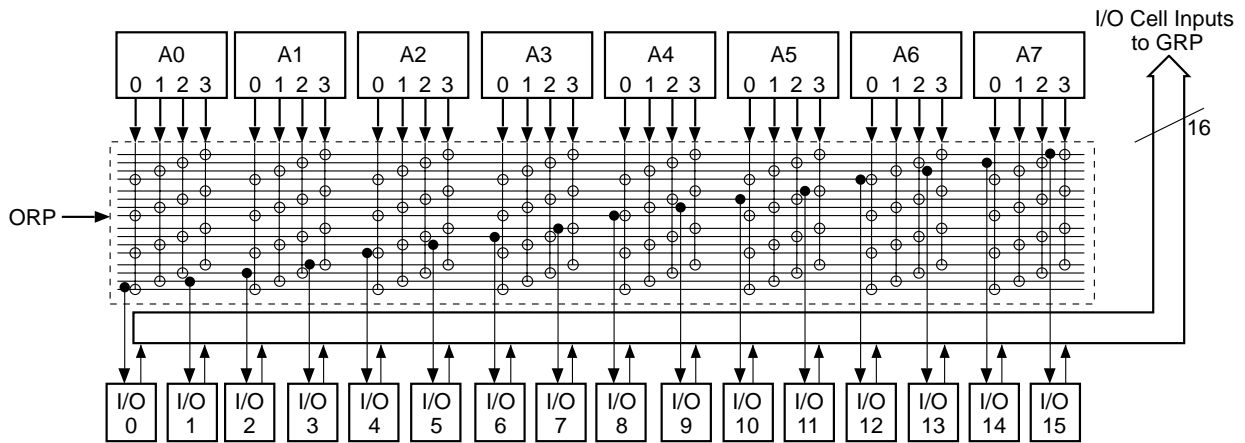
Figure 10. ispLSI 2000E, 2000VE and 2000VL Family Output Routing Pool Showing Bypass (Half I/O Versions)
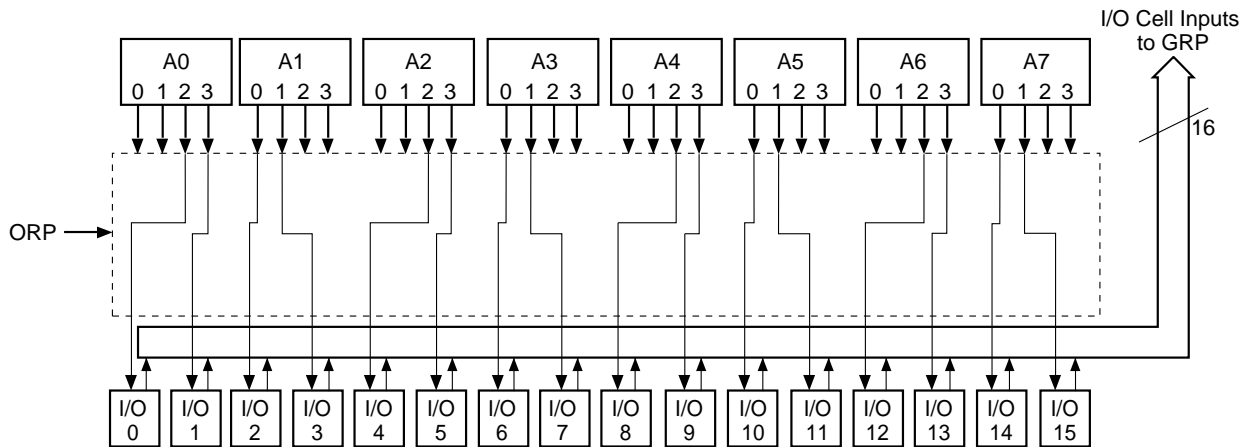
I/O Cell

Each I/O cell (Figure 11) can be individually programmed to be a combinatorial input, combinatorial output, or a bidirectional I/O pin with 3-state control. The product term output enable (PTOE) signal is still generated within each GLB using product term 19. The PTOE is generated in one of the eight GLBs. In addition to the PTOE, there is a global output enable (GOE) pin which can control any of the device's 3-state output buffers. The multiplexing between the GOE and PTOE is illustrated in Figure 11. The 2032 architecture has one GOE and the 2064, 2096 and 2128 architectures each have two GOEs.

Output buffers contain a fuse-programmable slew rate control. In addition to the standard output configuration,

the outputs of the ispLSI 2000E, 2000VE and 2000VL families are individually programmable either as standard totem-pole or open-drain outputs.

Two new features in the ispLSI 2000E Family include user-selectable 3.3V or 5V I/O, and PCI compatible outputs. These options are not available in 44-pin packages.

A new feature added to the 2000VE and 2000VL families is Boundary Scan Test. All 2000VE and 2000VL family members are 100% IEEE 1149.1 Boundary Scan Testable through the Boundary Scan Test Access Port (TAP).

Figure 11. ispLSI 2000E, 2000VE and 2000VL Family I/O Cell Architecture

⊗ Represents an E^{2}CMOS Cell.
* Except 2032
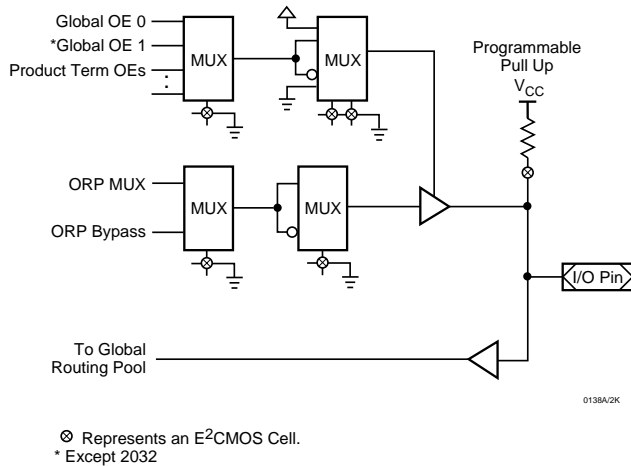
Figure 12. Examples of I/O Cell Configurations
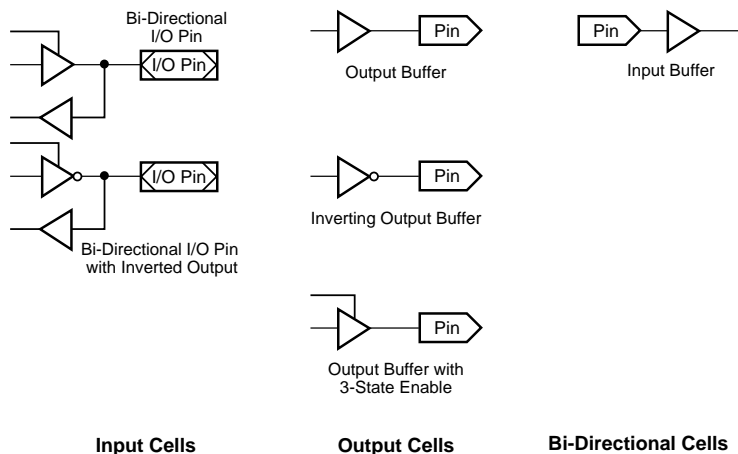
2000E, 2000VE and 2000VL Family Architectural Description

Global Routing Pool

The GRP is a Lattice proprietary interconnect structure which offers fast predictable speeds with complete connectivity. The GRP allows the outputs from the GLBs or the I/O cell inputs to be connected to the inputs of the GLBs. Any GLB output is available to the input of all other GLBs, and similarly an input from an I/O pin is available as an input to all of the GLBs. Because of the uniform architecture of the ispLSI devices, the delays through the GRP are both consistent and predictable. However, they are slightly affected by GLB loading.

Clock Distribution

The Global Clock Distribution is shown in Figure 19. The three global clock signals, CLK 0, CLK 1 and CLK 2 are generated from the three dedicated global clock input pins, Y0, Y1 and Y2. The three global clocks, CLK 0, CLK 1 and CLK 2 are used for clocking all the GLBs in the device.
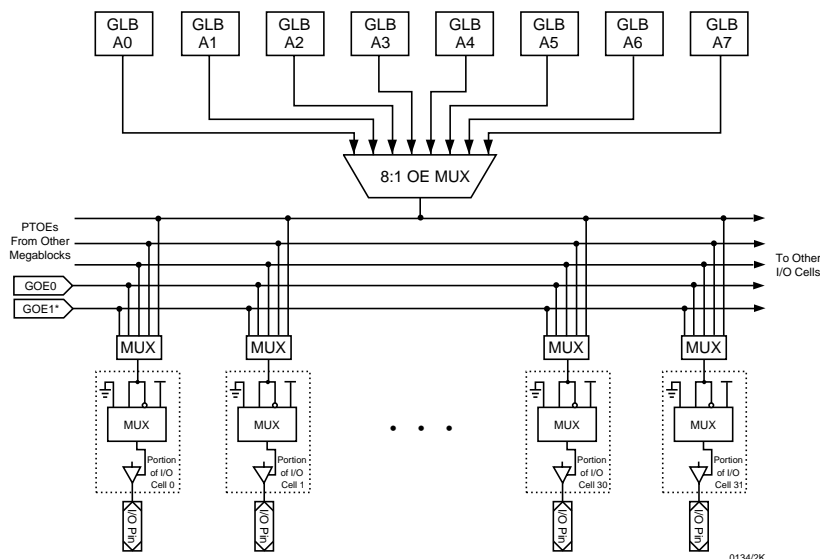
All GLBs have the capability of generating their own asynchronous clocks using the clock Product Term (PT12). CLK 0, CLK 1 and CLK 2 feed to the corresponding clock MUX inputs on all the GLBs (Figure 2).

Output Enable Control

One PTOE signal can be generated within each GLB using the PTOE Product Term (PT19). One of the eight PTOE signals within a Megablock is then routed to all of the I/O cells within that Megablock (Figure 13). This PTOE signal can simultaneously control any or all of the I/O cells which are used in 3-state mode. (Individual I/O cells also have independent control for permanently enabling or disabling the output buffer). In this way, one PTOE signal is generated by each Megablock for 3-state operation. The advantage to this approach is that the PTOE signal can be generated in any GLB within the Megablock which happens to have an unused PTOE product term. This frees up the other PTOE product terms for use as logic. The one PTOE signal generated by each Megablock is made available to all the other I/O cells in the device, not only those in the same Megablock.

In addition to the PTOE there are dedicated Global OEs (GOE) in the devices. There is one GOE in the 2032 families, and two in each of the 2064, 2096, 2128 and 2192 families. The GOE signals run to all the I/O cells in the device. Any GOE can be selected as the Output Enable to control any or all of the I/O cells in the device.

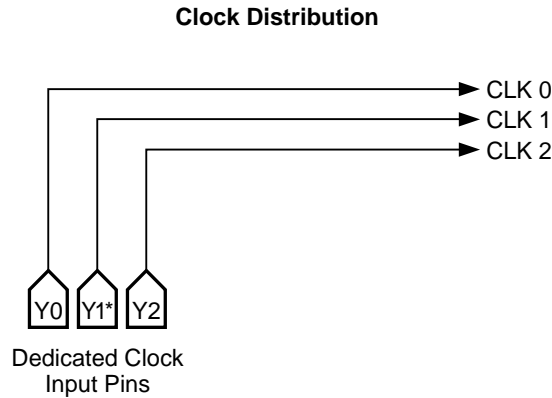Figure 13. ispLSI 2000E, 2000VE and 2000VL Family Output Enable Controls

* Except 2032

Figure 14. Global Clock Structure

Clock Distribution

CLK 0
CLK 1
CLK 2

Y0 Y1* Y2

Dedicated Clock
Input Pins

*Note: Y1 and $\overline{RESET}$ and Y2 and SCLK are multiplexed (44 and 48-pin devices).
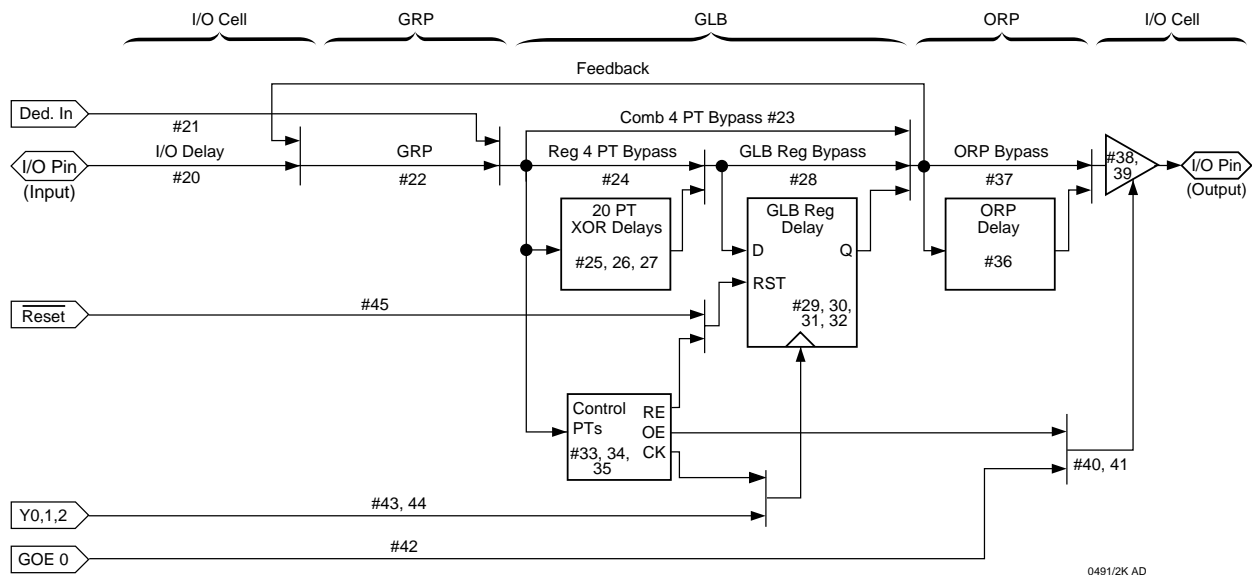
0095A3isp/2K

Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in Figure 15. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow and add the various delays together (Figure 15). Critical timing paths are shown in Figure 15, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. External timing parameters are tested and guaranteed on every device.

Figure 15. ispLSI 2032VE Timing Model

| I/O Cell | GRP | GLB | ORP | I/O Cell |

Feedback

Ded. In
#21

Comb 4 PT Bypass #23

I/O Pin (Input)
I/O Delay
#20

GRP
#22

Reg 4 PT Bypass
#24

GLB Reg Bypass
#28

ORP Bypass
#37

#38, 39

I/O Pin (Output)

20 PT XOR Delays
#25, 26, 27

GLB Reg Delay
D   Q
RST
#29, 30, 31, 32

ORP Delay
#36

Reset
#45

Control PTs
#33, 34, 35
RE
OE
CK

#40, 41

Y0,1,2
#43, 44

GOE 0
#42

0491/2K AD

Derivations of $t$su, th and $t$co from the Product Term Clock

$t$su   = Logic + Reg su - Clock (min)
          = ($t$io + $t$grp + t20ptxor) + ($t$gsu) - ($t$io + $t$grp + $t$ptck(min))
          = (#20 + #22 + #26) + (#29) - (#20 + #22 + #35)
   2.0ns = (0.4 + 0.6 + 1.9) + (0.5) - (0.4 + 0.6 + 0.4)

th   = Clock (max) + Reg h - Logic
          = ($t$io + $t$grp + $t$ptck(max)) + ($t$gh) - ($t$io + $t$grp + t20ptxor)
          = (#20 + #22 + #35) + (#30) - (#20 + #22 + #26)
   1.9ns = (0.4 + 0.6 + 2.3) + (1.5) - (0.4 + 0.6 + 1.9)

$t$co   = Clock (max) + Reg co + Output
          = ($t$io + $t$grp + $t$ptck(max)) + ($t$gco) + ($t$orp + $t$ob)
          = (#20 + #22 + #35) + (#31) + (#36 + #38)
   5.2ns = (0.4 + 0.6 + 2.3) + (0.3) + (0.6 + 1.0)

Note: Calculations are based on timing specifications for the ispLSI 2032VE-300L.

Table 2-0042/2032VE