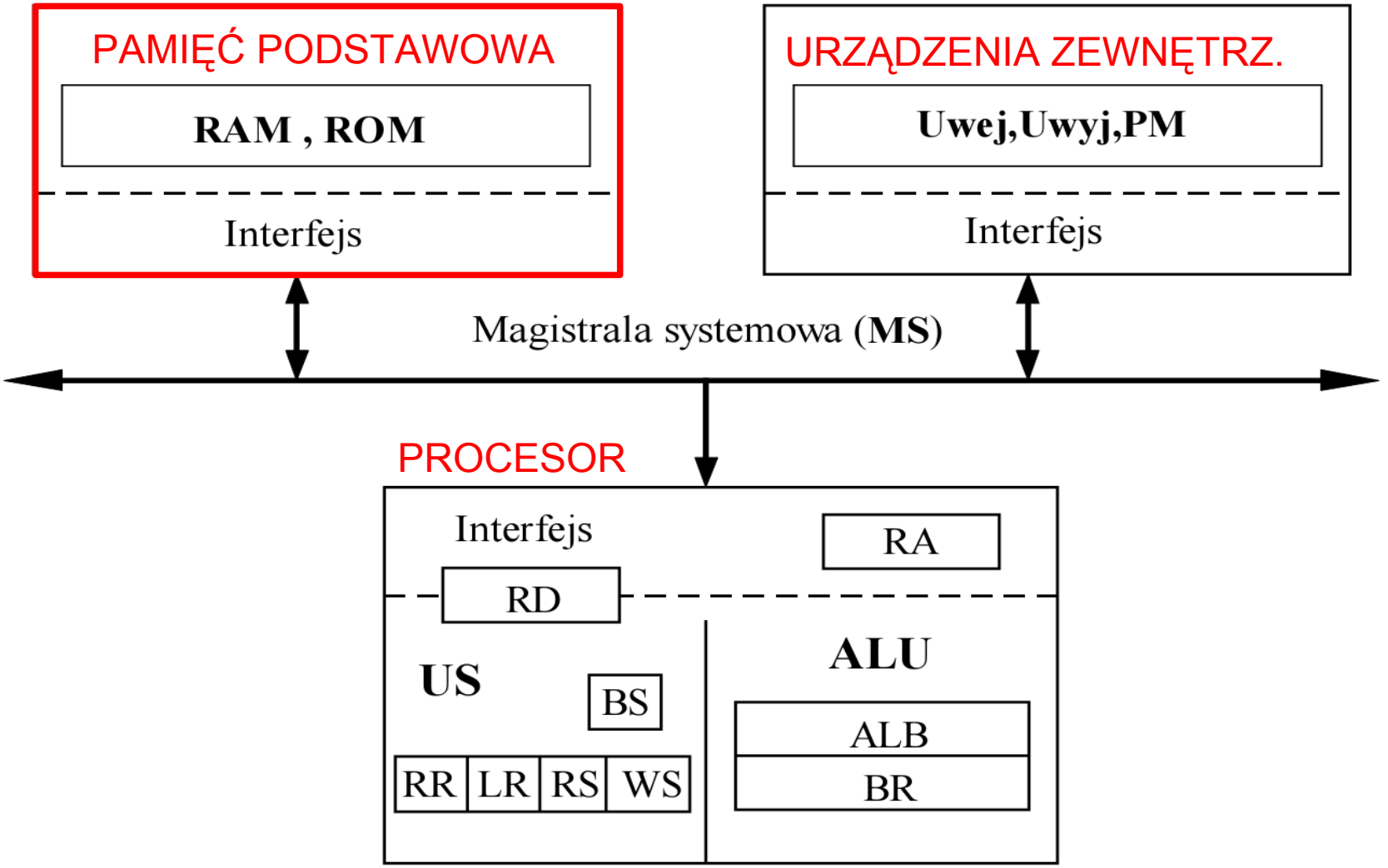
Zakres przedmiotu

1. Wstęp do systemów mikroprocesorowych.
2. **Współpraca procesora z pamięcią. Pamięci półprzewodnikowe.**
3. Architektura systemów mikroprocesorowych.
4. Współpraca procesora z urządzeniami peryferyjnymi.
5. Przykładowy system mikroprocesorowy.
6. Architektura procesorów 32-bitowych na przykładzie układów Freescale 68k/ColdFire.
7. Architektura mikrokontrolerów 8-bitowych.

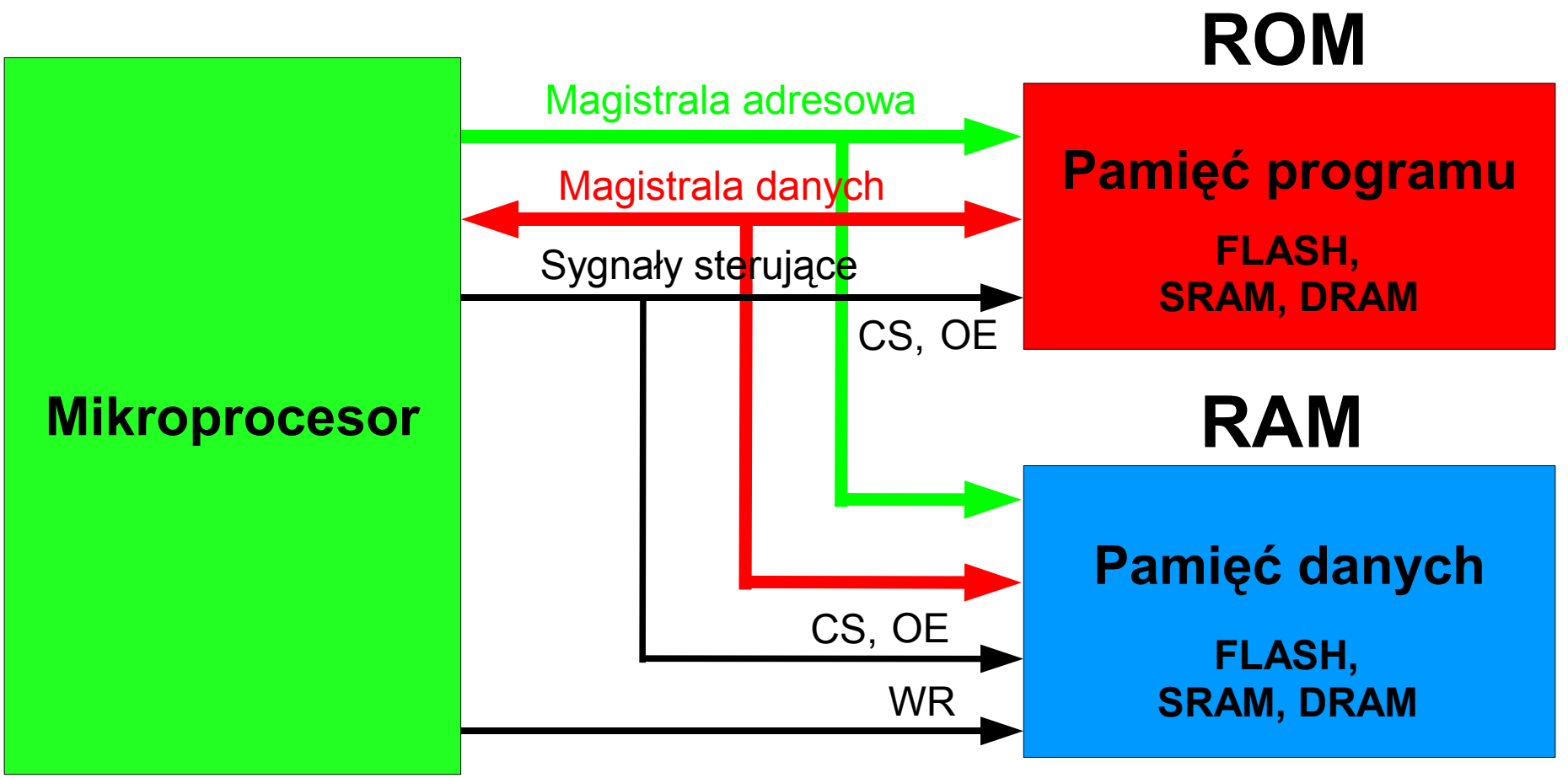
Architektura systemu komputerowego

Architektura polega na ścisłym podziale komputera na trzy podstawowe części:

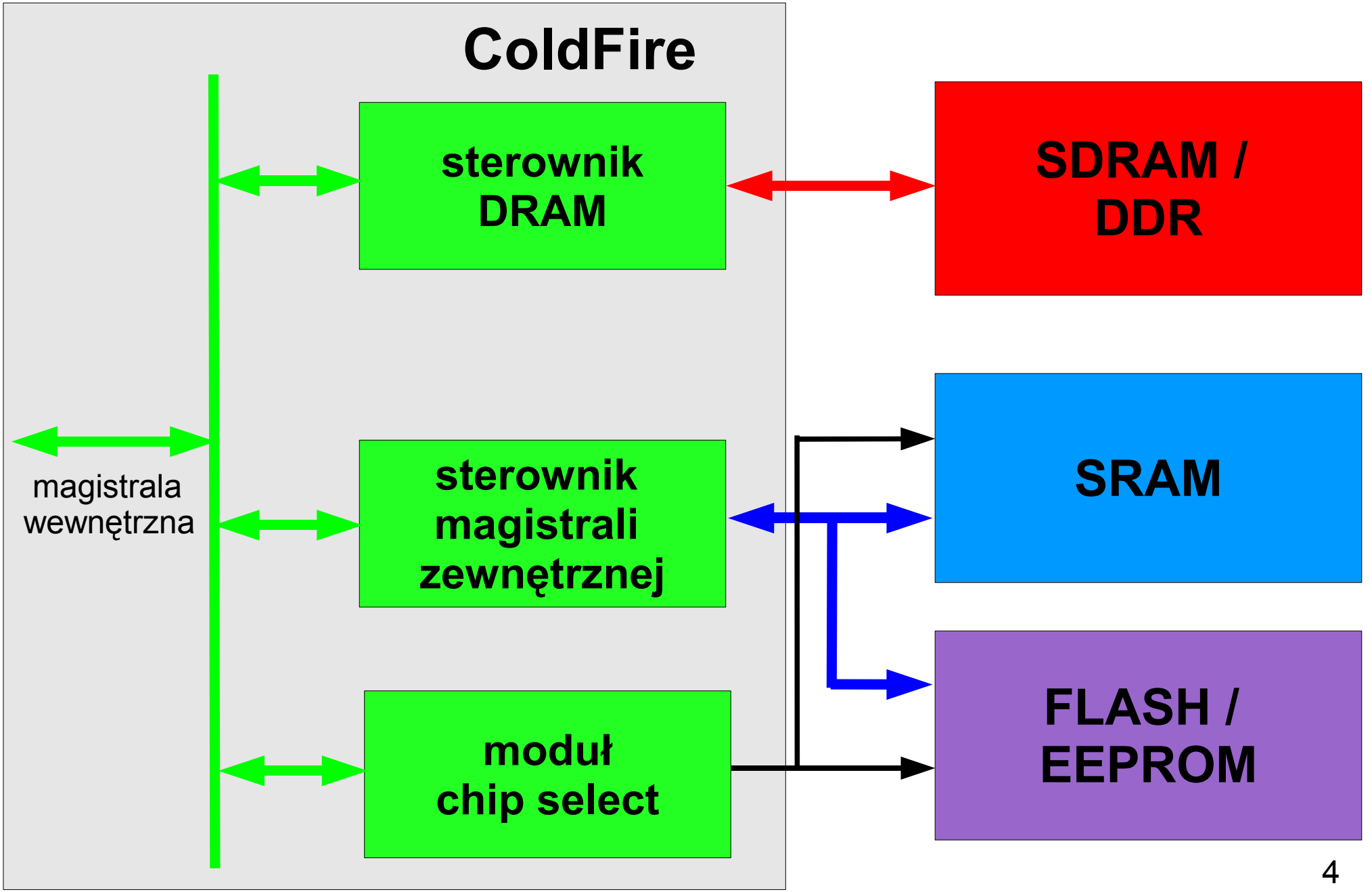
- procesor,
- pamięć (zawierająca dane oraz program),
- urządzenia wejścia/wyjścia (I/O).



Współpraca procesora z pamięcią zewnętrzną (1)



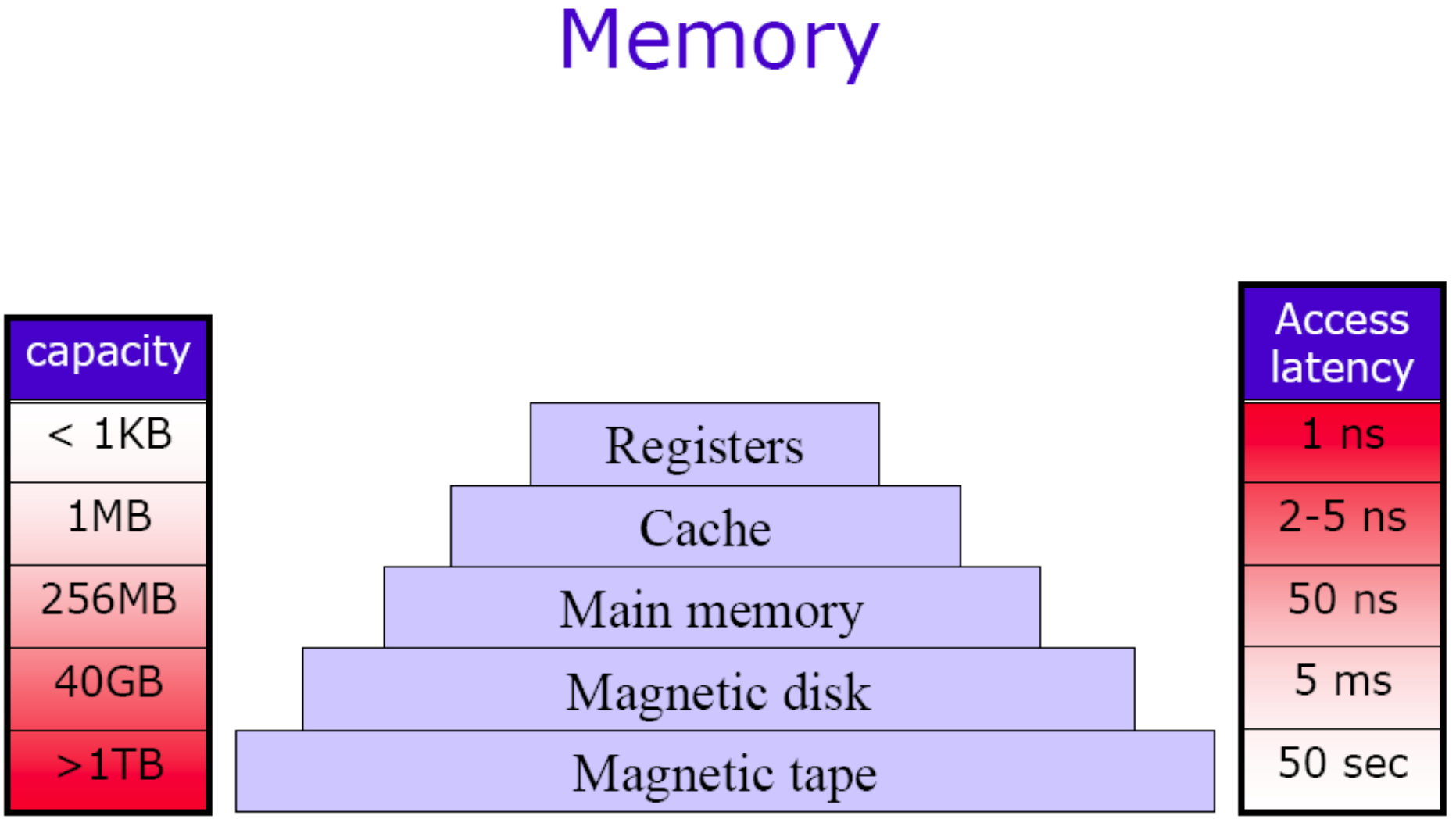
Współpraca procesora z pamięcią zewnętrzną (2)



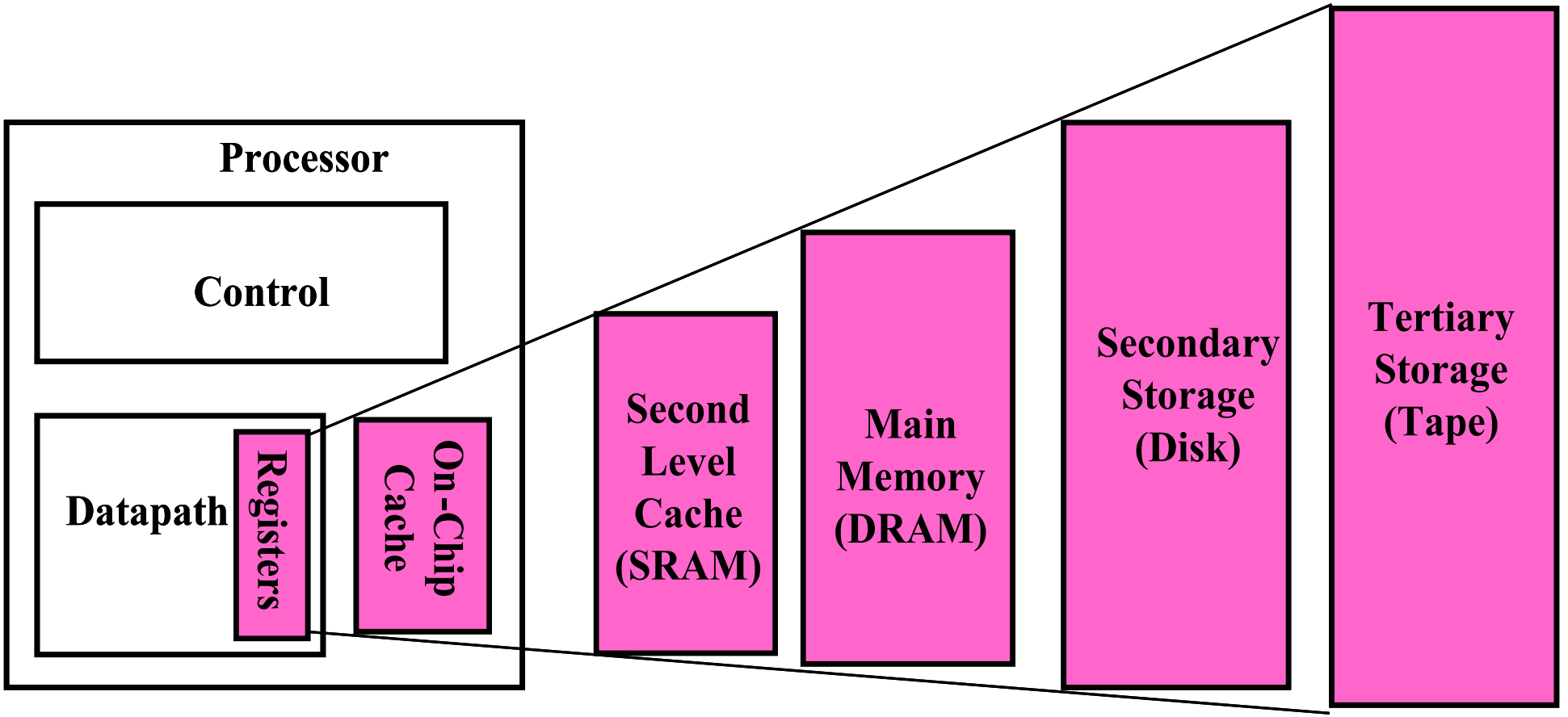
Podział pamięci

<table>
<tr><th colspan="2">Pamięci ulotne</th><th>Pamięci nieulotne</th></tr>
<tr><th>Pamięci o dostępie swobodnym
RAM</th><th>Pamięci
bez swobodnego
dostępu</th><th rowspan="2">■ programowane maską – ROM
■ programowane jednorazowo – PROM
■ kasowalne i programowalne wielokrotnie – EPROM
■ elektrycznie kasowalne i programowalne wielokrotnie – EEPROM
■ elektrycznie kasowalne w całości i programowalne wielokrotnie – FLASH
■ pamięci S-RAM z podtrzymującą baterią litową</th></tr>
<tr><td>■ statyczne S-RAM
■ dynamiczne D-RAM</td><td>■ stosowe – LIFO
■ kolejkowe – FIFO
■ skojarzeniowe – CAM
■ rejestry przesuwające</td></tr>
</table>

Hierarchia pamięci (1)



Hierarchia pamięci (2)



Speed:	~1 ns	~10 ns-100 ns	~100 ns	~10 ms	~10 sec
Size:	~100 B	~kB-MB	~MB	~GB	~TB

Tera 10^12 => TB
Peta 10^15 => PB
Exa 10^18 => EB

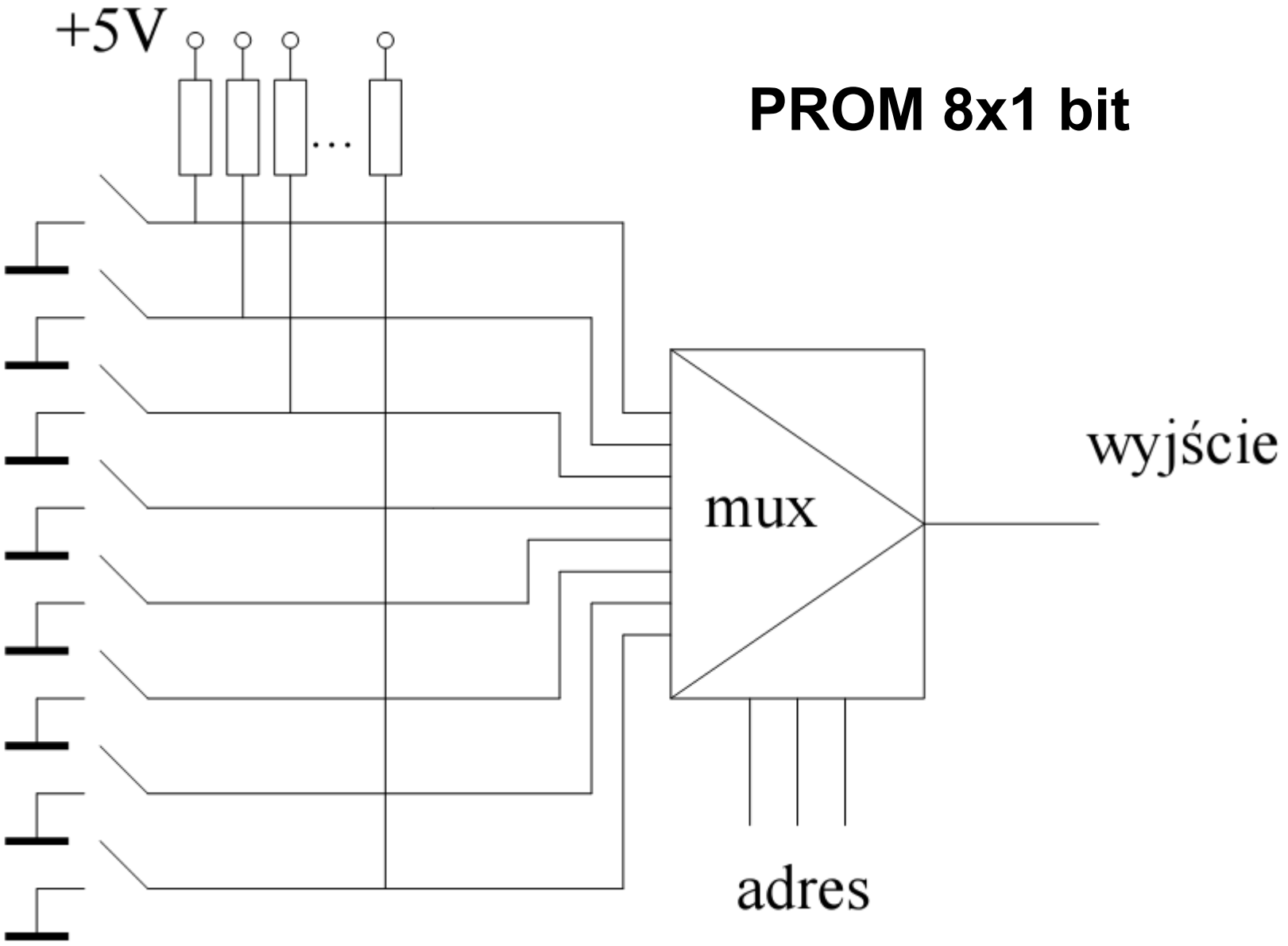
Pamięci tylko do odczytu (Read Only Memory)

Pamięci stałe ROM w systemach mikroprocesorowych

Pamięci ROM wykorzystuje się do:

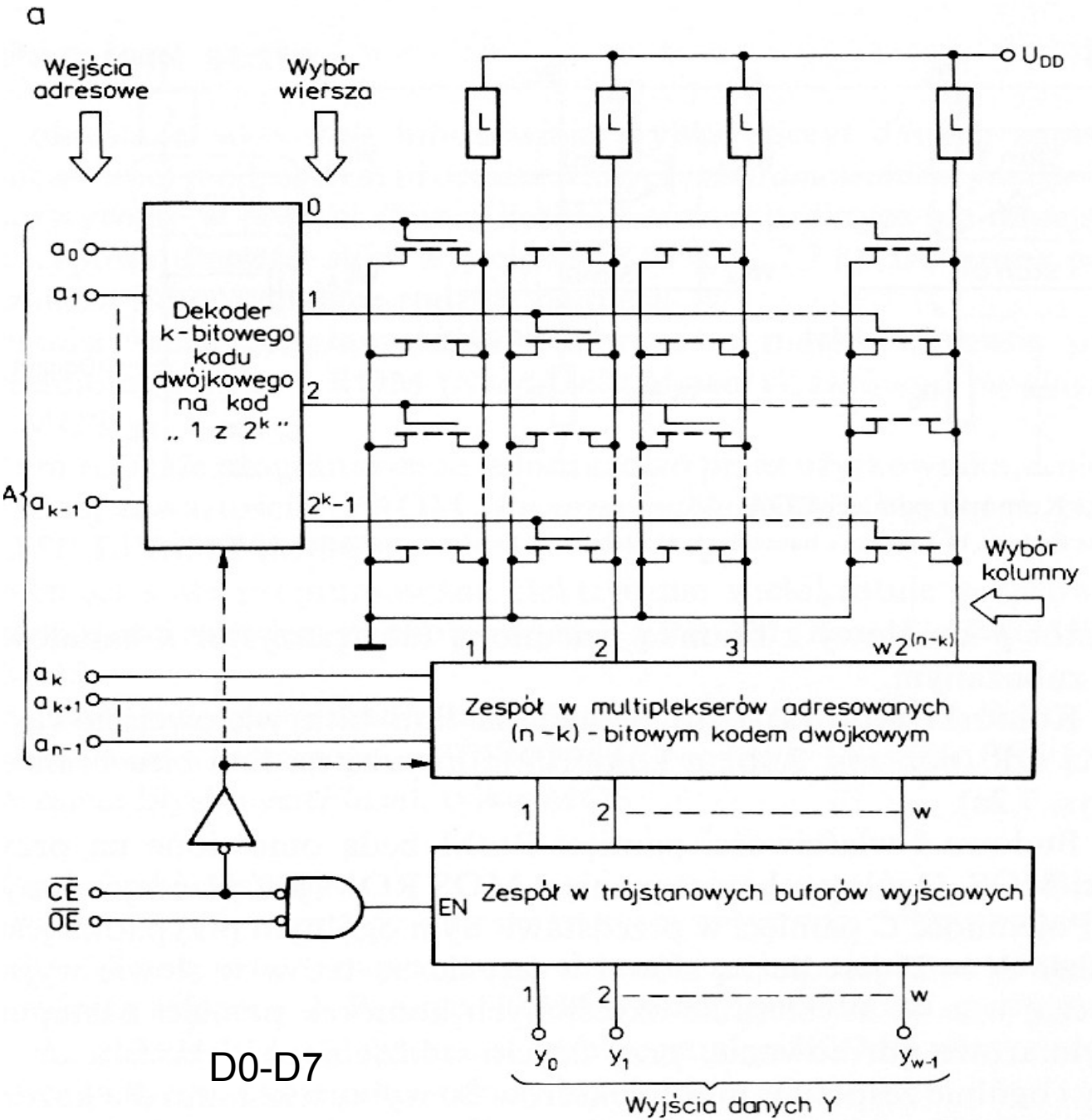
- Przechowywania programu,
- Budowy dekoderów adresowych
- Przechowywania stałych (parametrów)
- Przechowywania ustawień systemowych
- Realizacji funkcji nieliniowych, trygonometrycznych, itp., (np. tablicowanie)

Pamięć stała (1)



Pamięć stała (2)

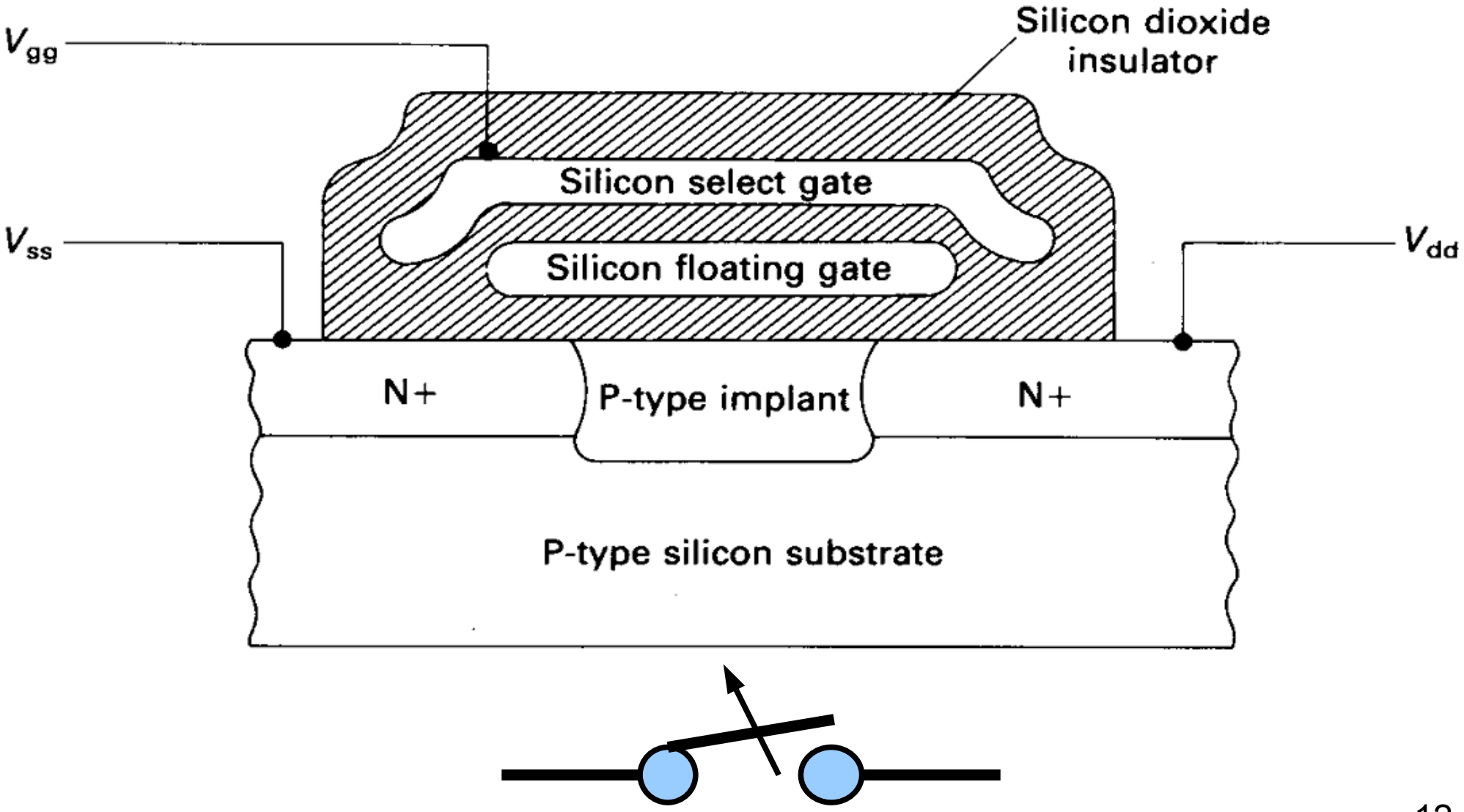
A0-A19 - 1MB



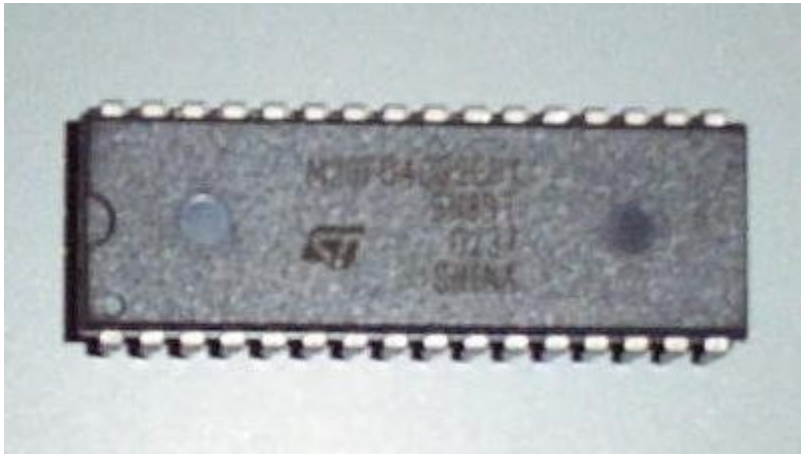
D0-D7

Pamięć EPROM

Structure of an EPROM memory cell

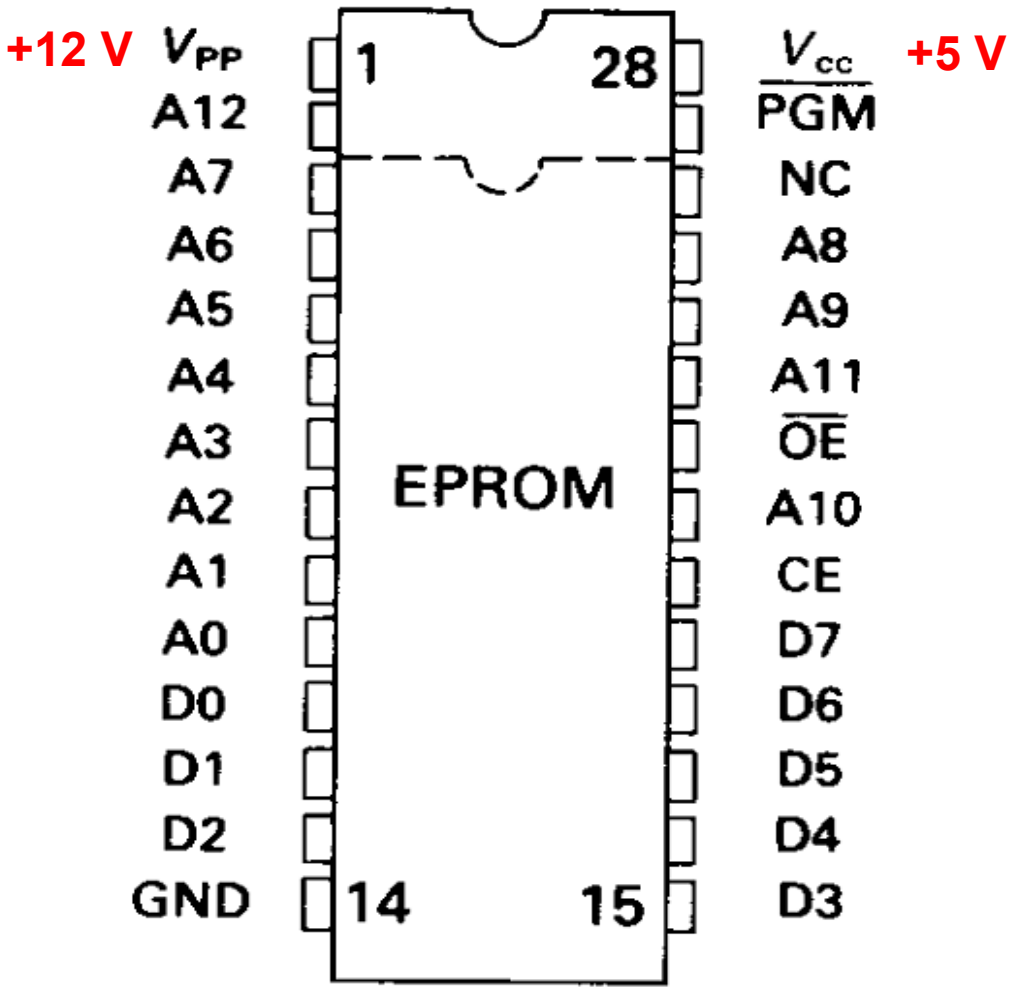


Pamięci EPROM



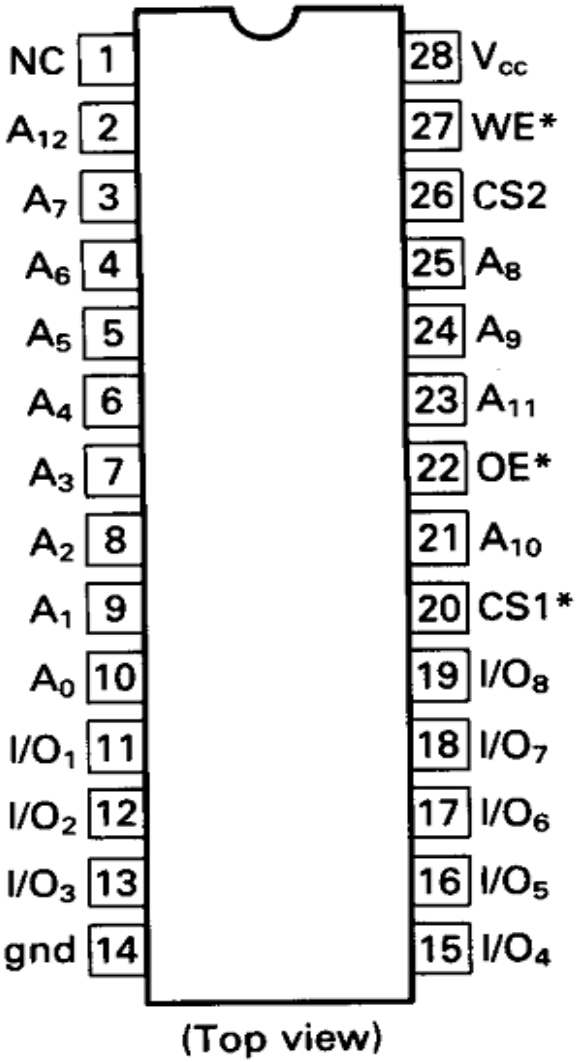
Pamięci EPROM / SRAM

2764



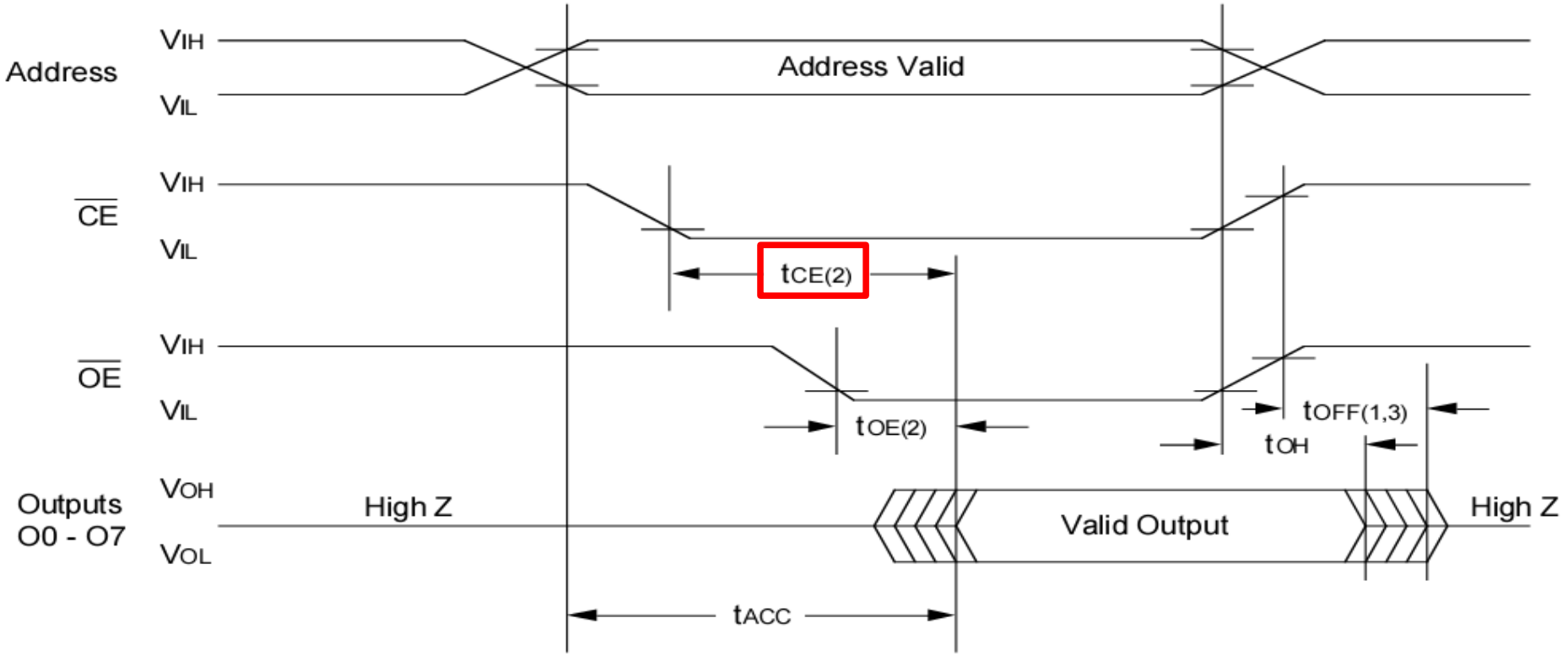
EPROM

6264



SRAM

Odczyt danej z pamięci EPROM

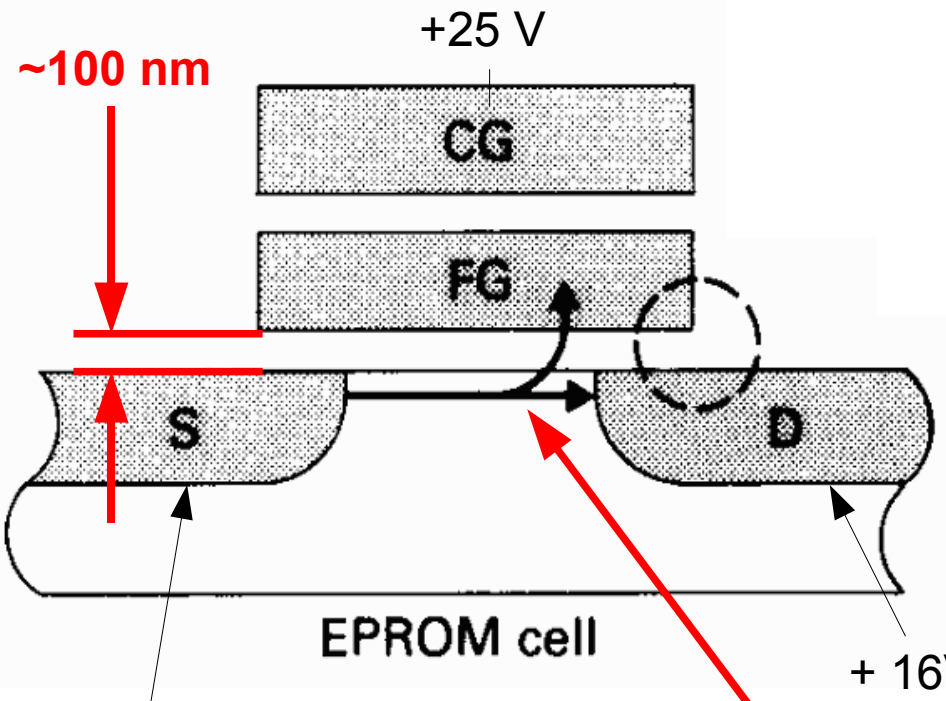


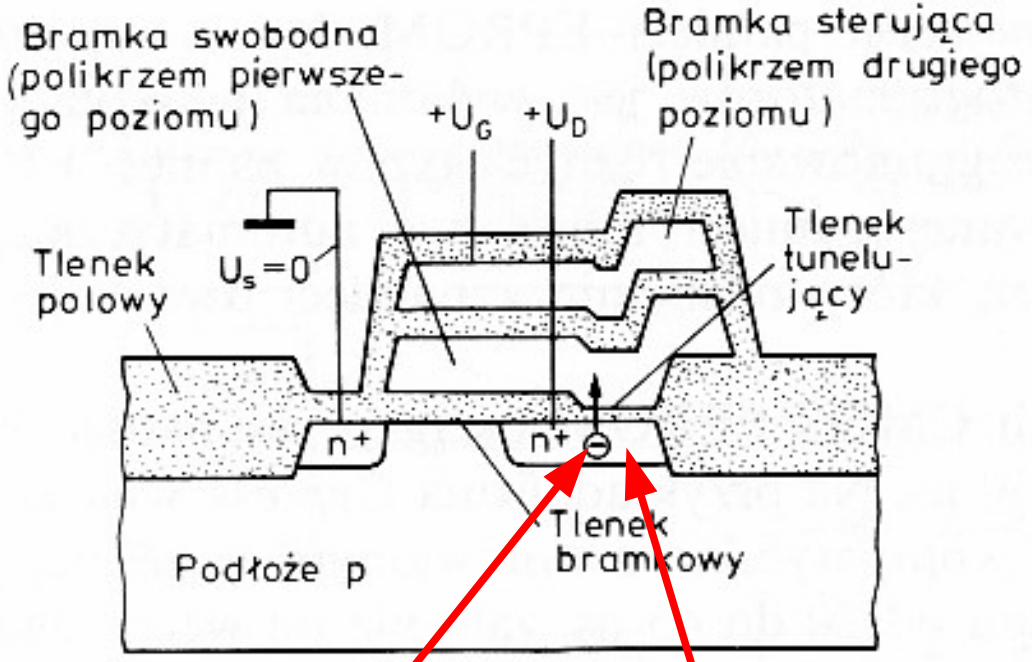
Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}$=$\overline{OE}$ =VIL
$\overline{CE}$ to Output Delay	tCE	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE}$ = VIL
$\overline{OE}$ to Output Delay	tOE	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE}$ = VIL
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

Pamięci EPROM <=> EEPROM

Structure of EPROM and flash EEPROM memory cells

CG — control gate
FG — floating gate
S — source
D — drain





Elektrony gorące: 10^5 V/cm

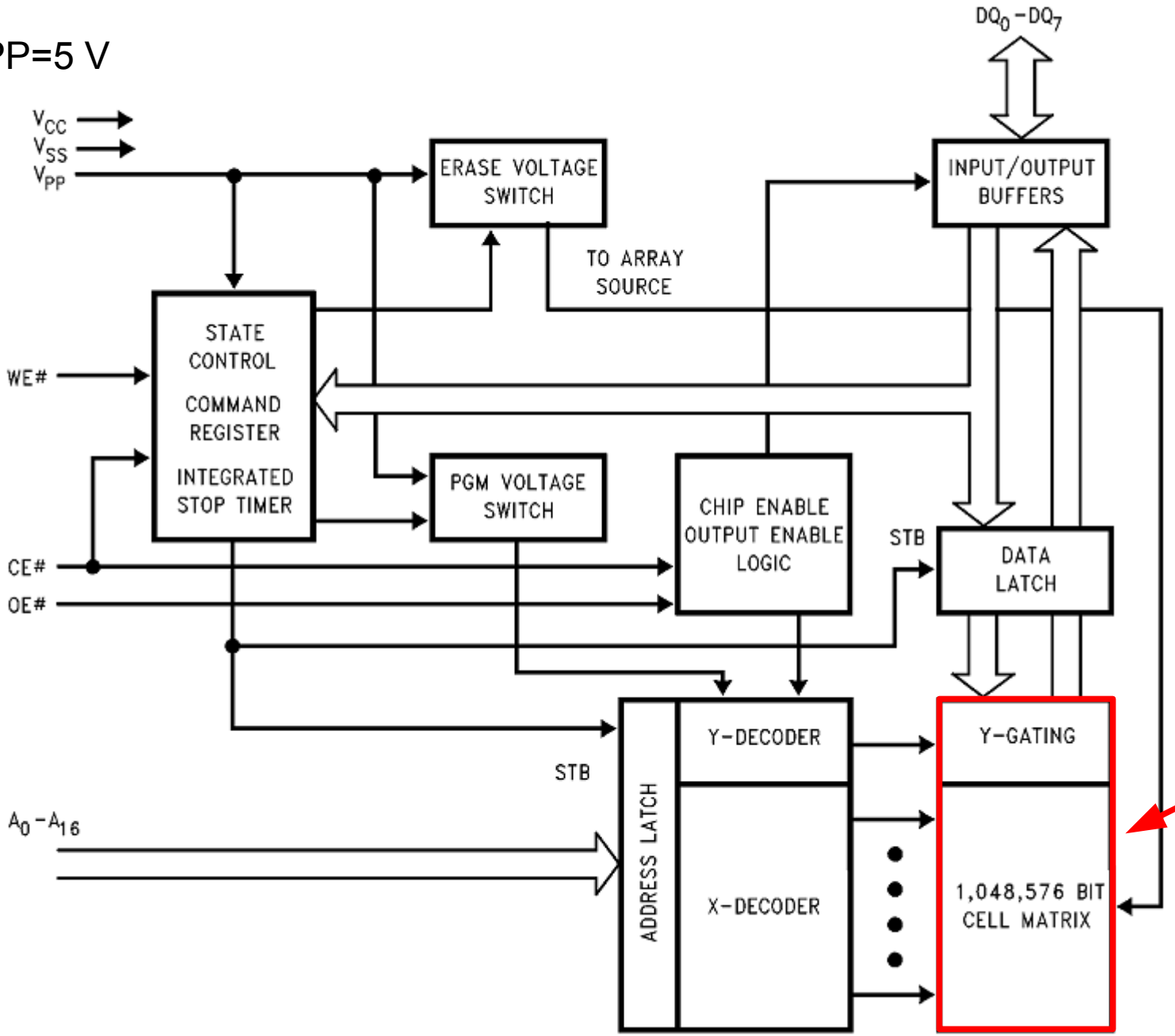
Kasowanie

Programowanie

Programowanie = wpisanie zer do komórek pamięci

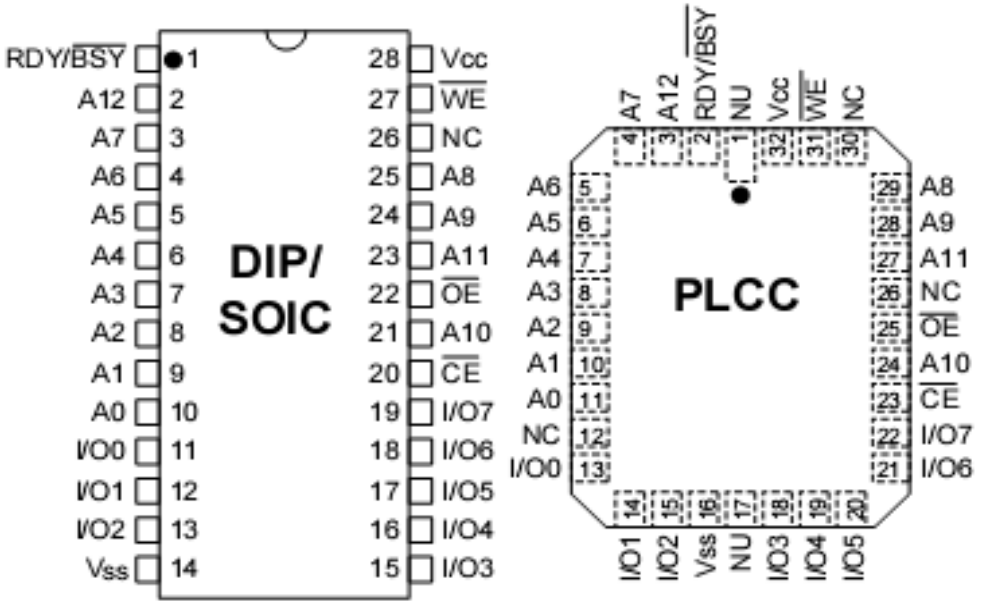
Pamięć EEPROM

VCC=VPP=5 V

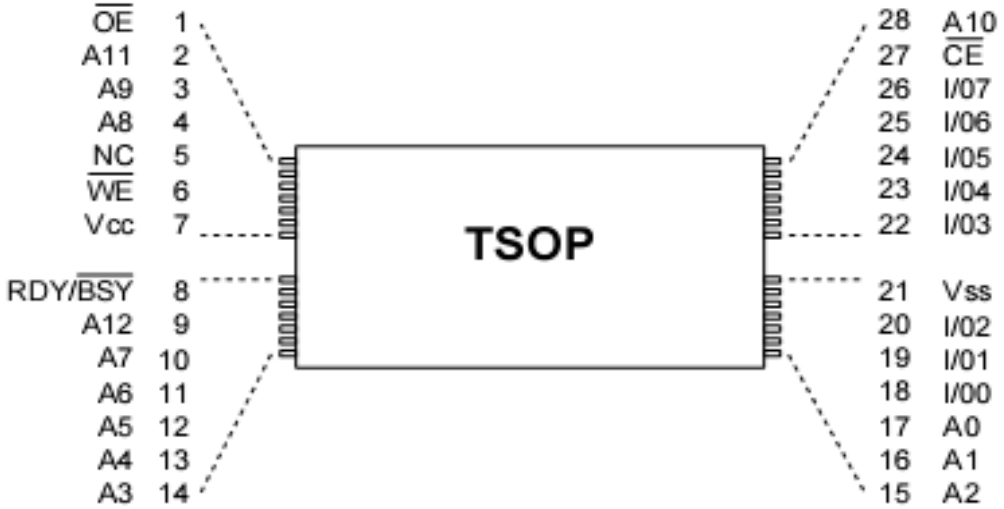


Matryca pamięci

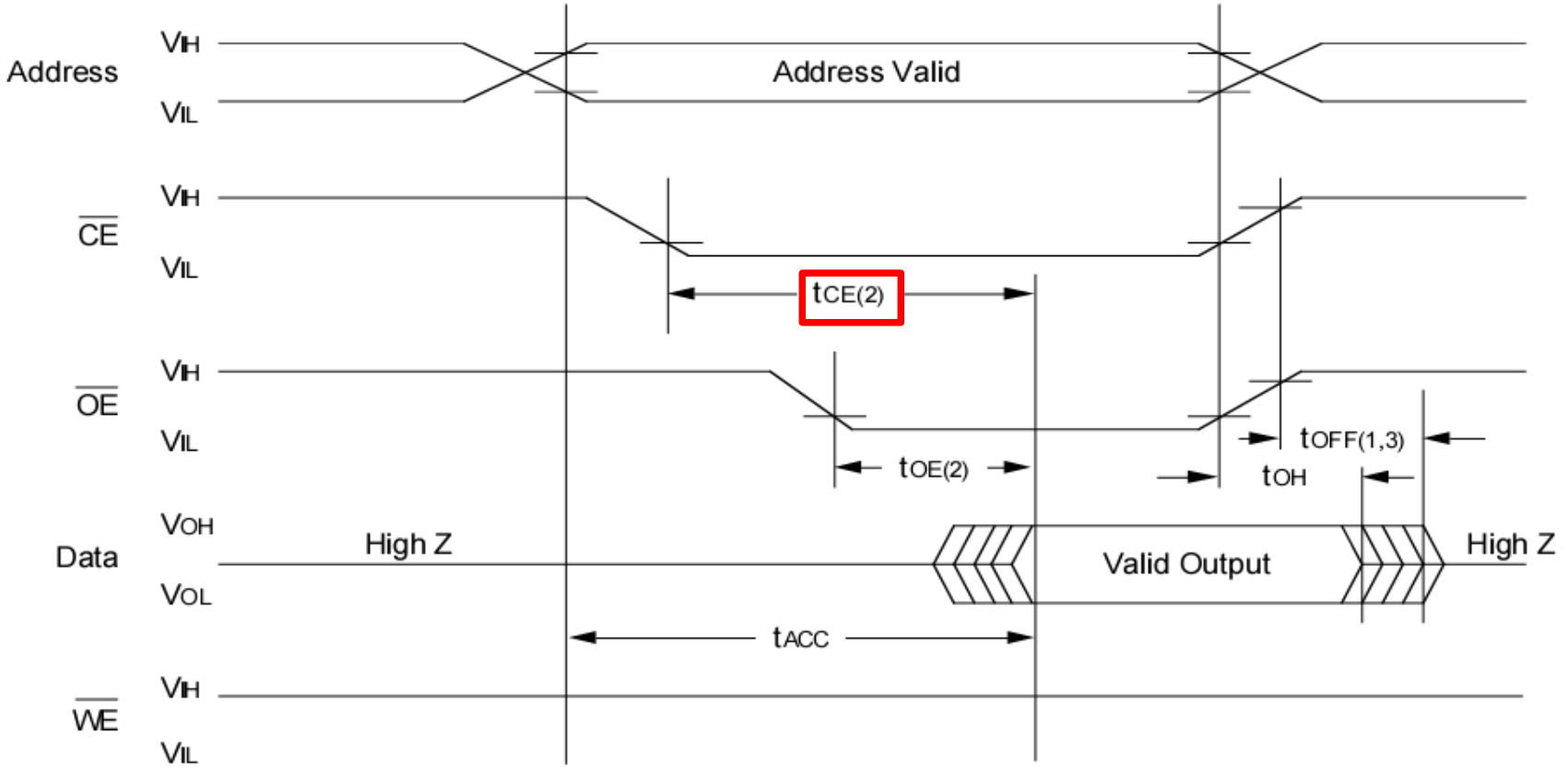
EEPROM 28C64A



● Pin 1 indicator on PLCC on top of package

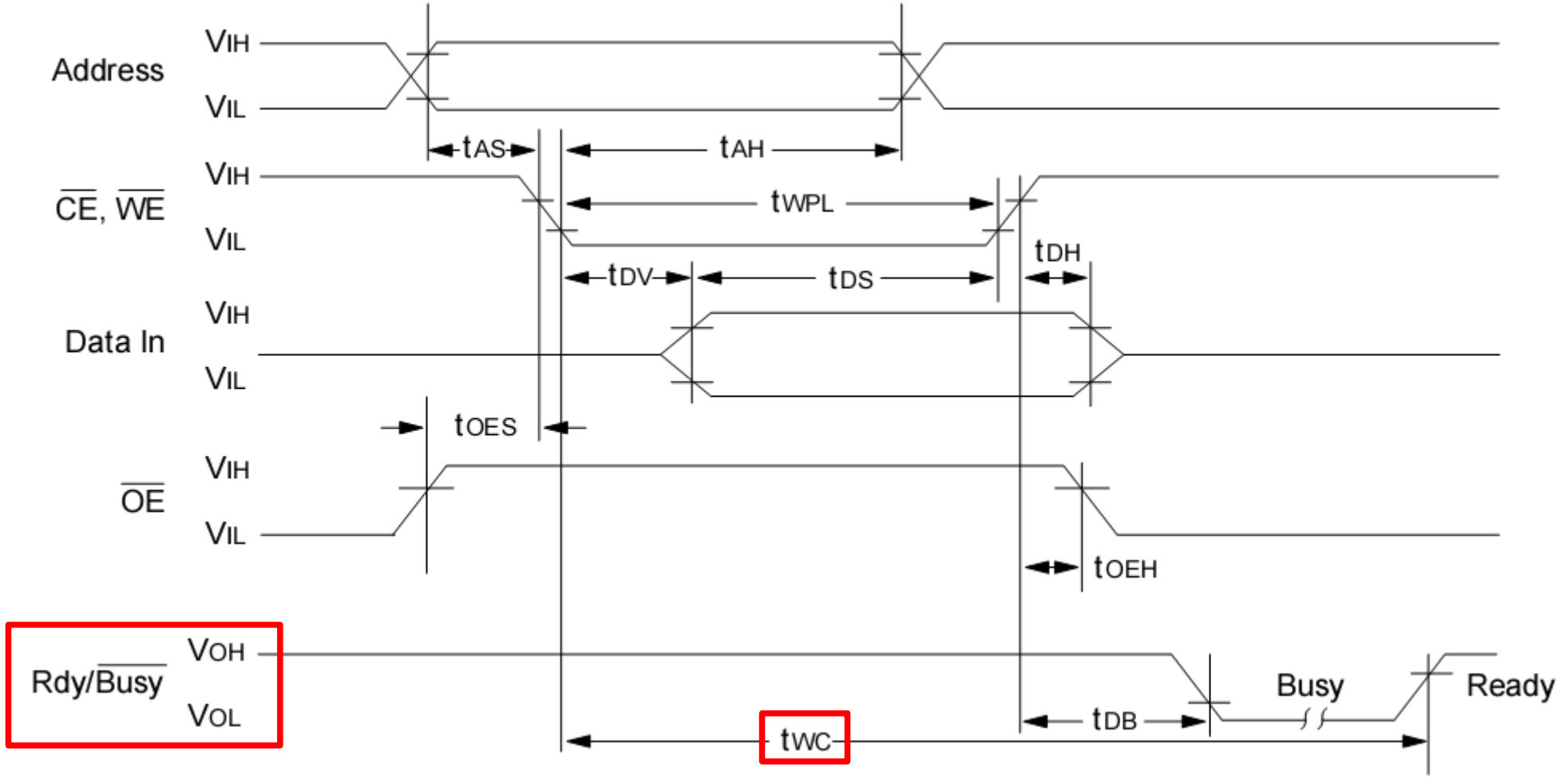


Odczyt pamięci EEPROM



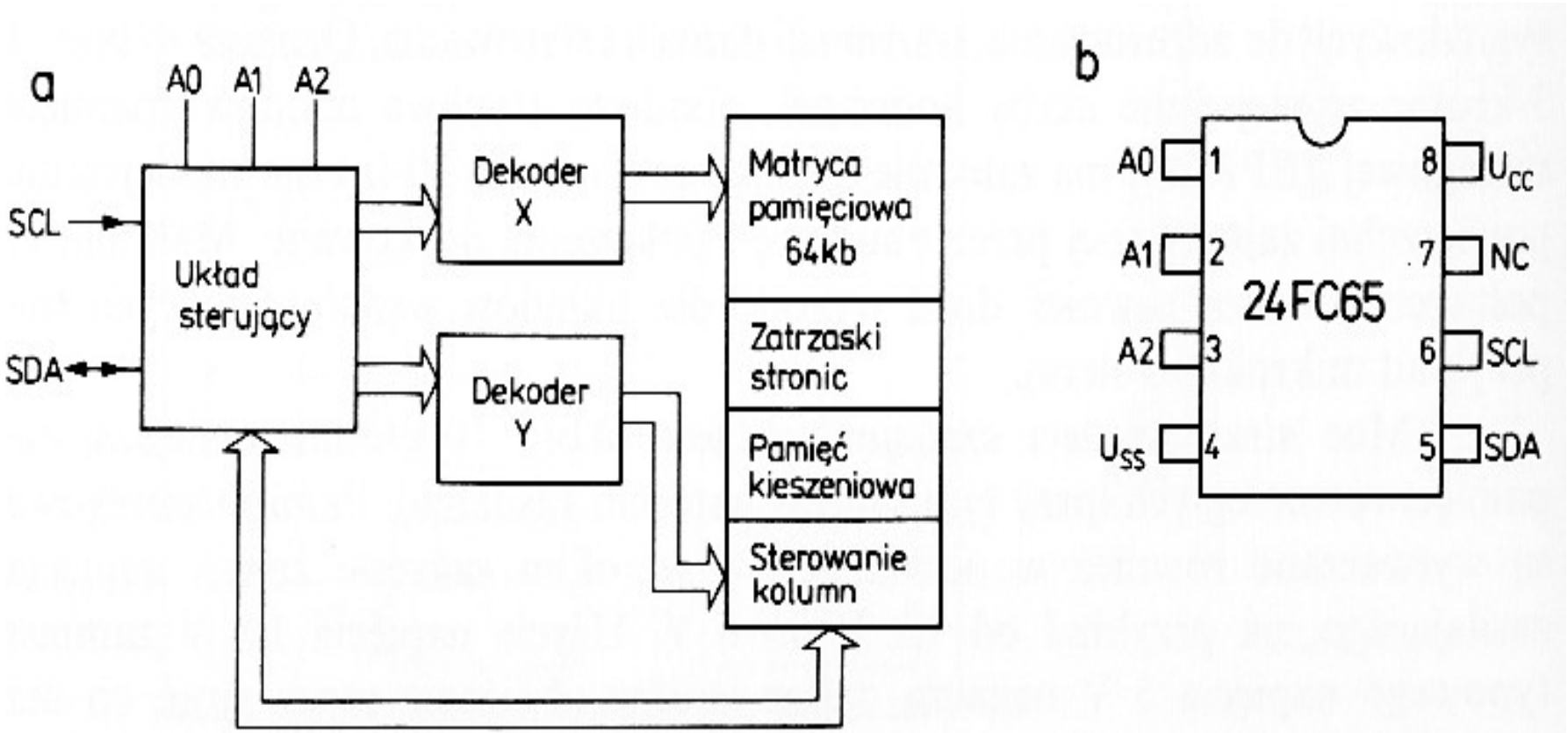
Parameter	Symbol	28C64A-15		28C64A-20		28C64A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = VIL
$\overline{CE}$ to Output Delay	tCE	—	150	—	200	—	250	ns	$\overline{OE}$ = VIL
$\overline{OE}$ to Output Delay	tOE	—	70	—	80	—	100	ns	$\overline{CE}$ = VIL
$\overline{CE}$ or $\overline{OE}$ High to Output Float	tOFF	0	50	0	55	0	70	ns	Note 1
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	tOH	0	—	0	—	0	—	ns	Note 1

Zapis pamięci EEPROM



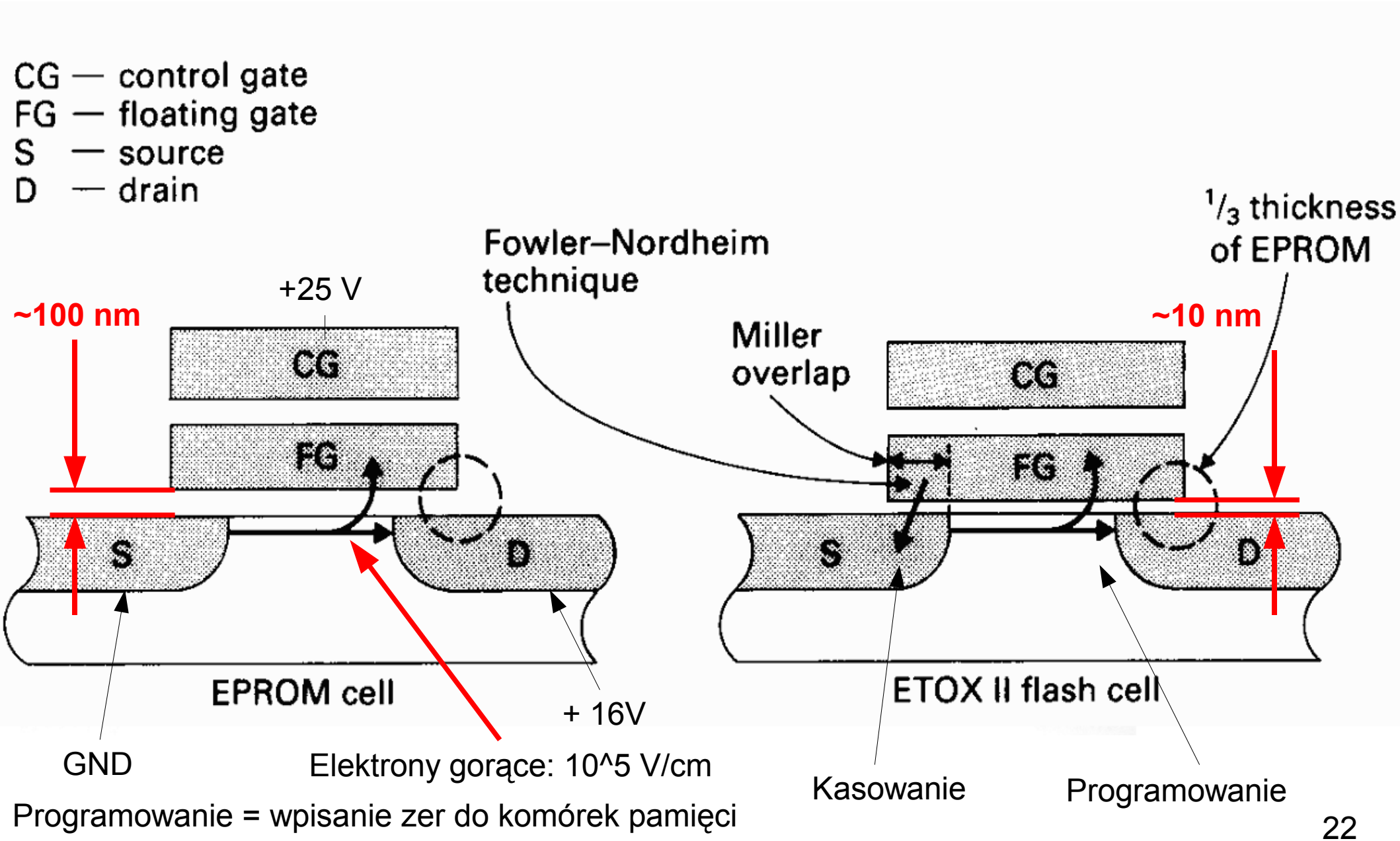
Parameter	Symbol	Min	Max	Units	Remarks
Time to Device Busy	tDB	2	50	ns	
Write Cycle Time (28C64A)	tWC	—	1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	tWC	—	200	µs	100 µs typical

Pamięć EEPROM z interfejsem I^2C



Niewielka pamięć z interfejsem szeregowym 8k x 8 = 64 kb

Pamięci EPROM <=> FLASH



Programowanie = wpisanie zer do komórek pamięci

Pamięci FLASH (1)

Zalety:

- Możliwość szybkiego kasowania sektorów (bloków) pamięci,
- Duża pojemność pamięci (jednotranzystorowe komórki),
- Niskie napięcie zasilania (3,3 V, 5 V),
- Niewielki czas odczytu danych (~10 ns).
- Niewielkie rozmiary,
- Duża odporność na wstrząsy,
- Mały pobór energii.

Wady:

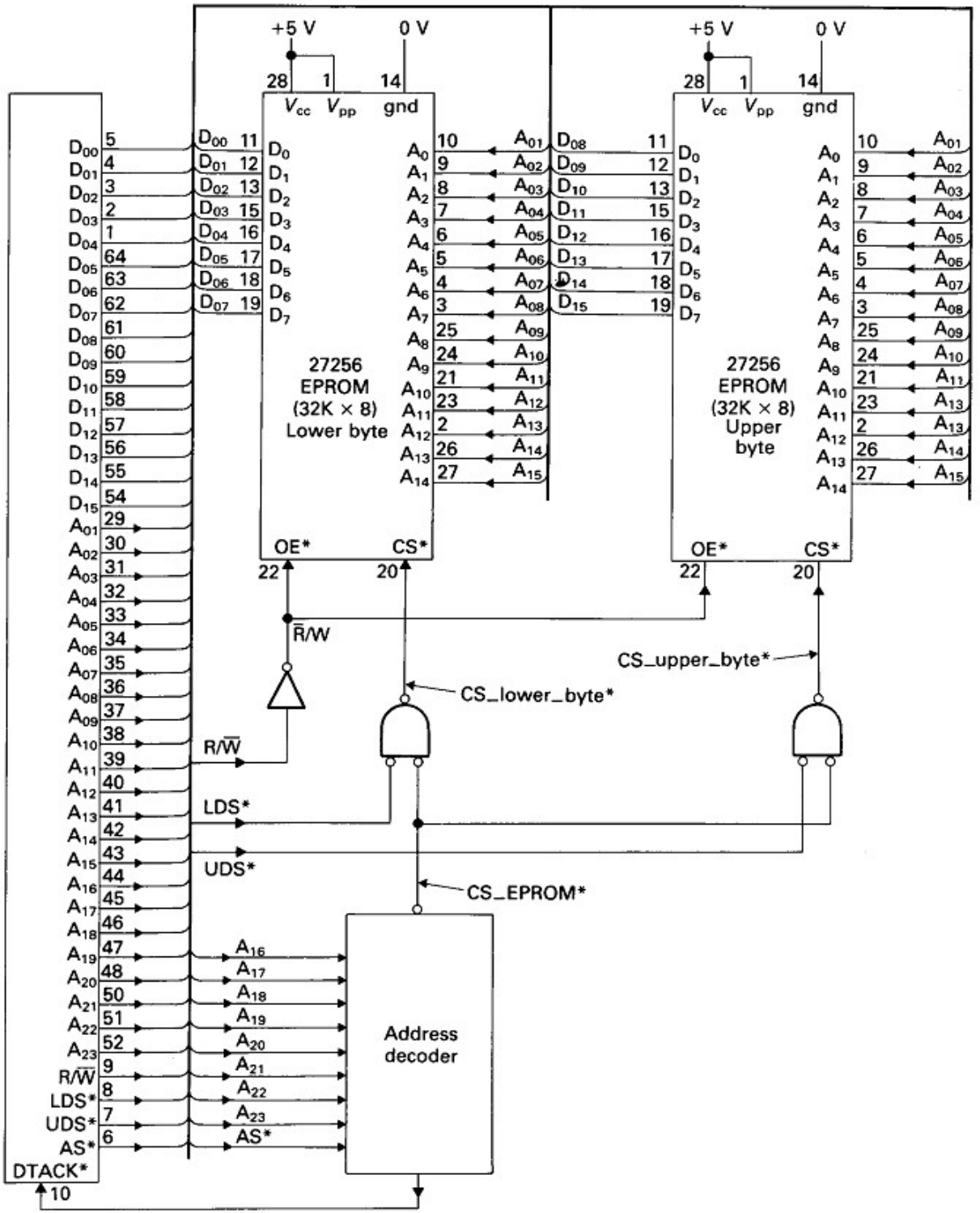
- Brak możliwości kasowania pojedynczych bajtów.

Pamięci FLASH (2)

Kasowanie zawartości pamięci

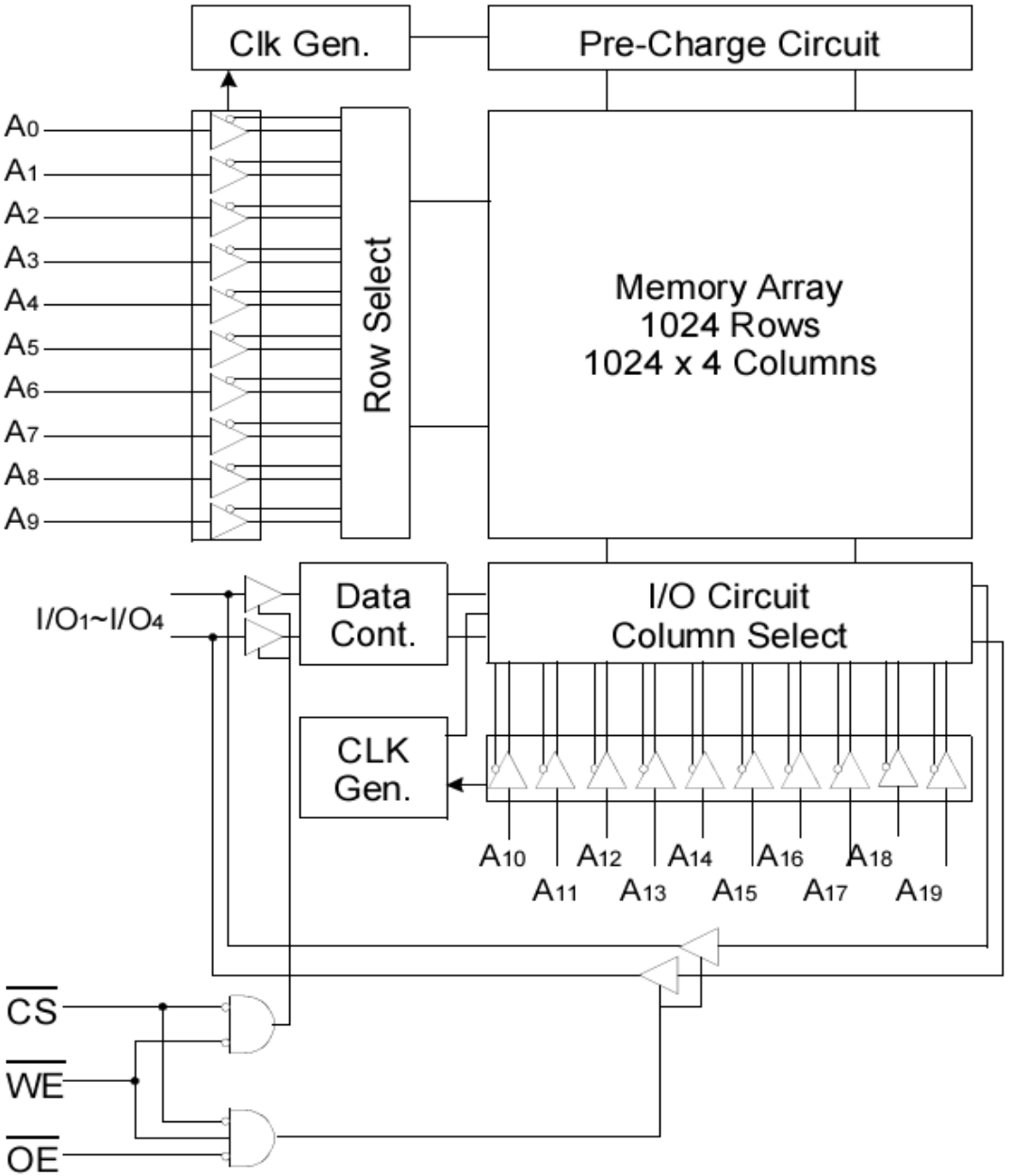
- PROM - niemożliwe
- EPROM - ultrafiolet (cała pamięć, ok. 20 min)
- EEPROM - elektrycznie (cała pamięć lub pojedyncze bloki, kasowane poprzez specyficzną sekwencję)
- Flash EEPROM - podobne jak EEPROM

Connecting a 27256 EPROM to a 68000 CPU



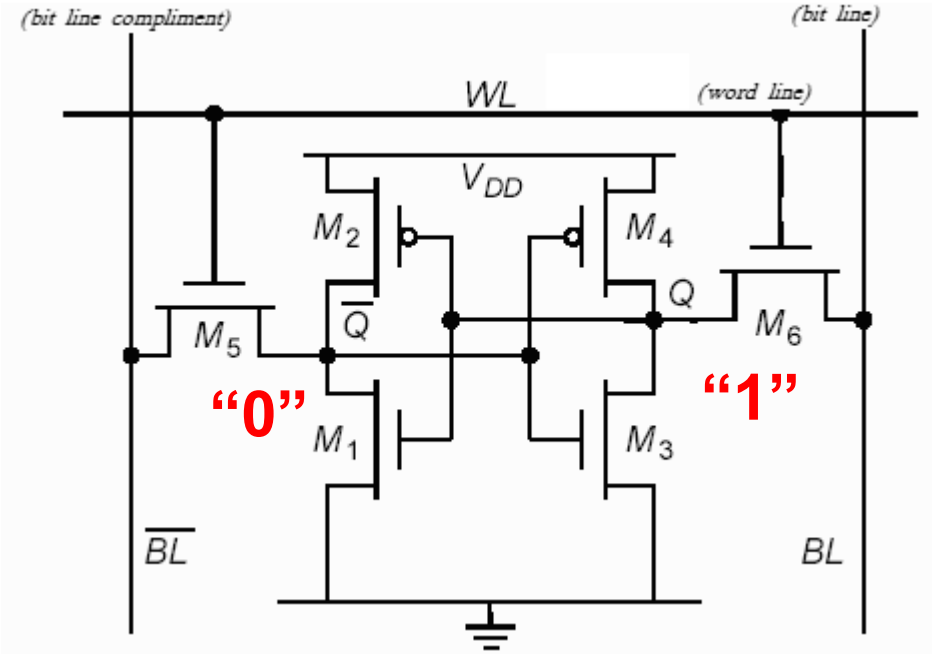
Pamięci o dostępie swobodnym (Random Access Memory)

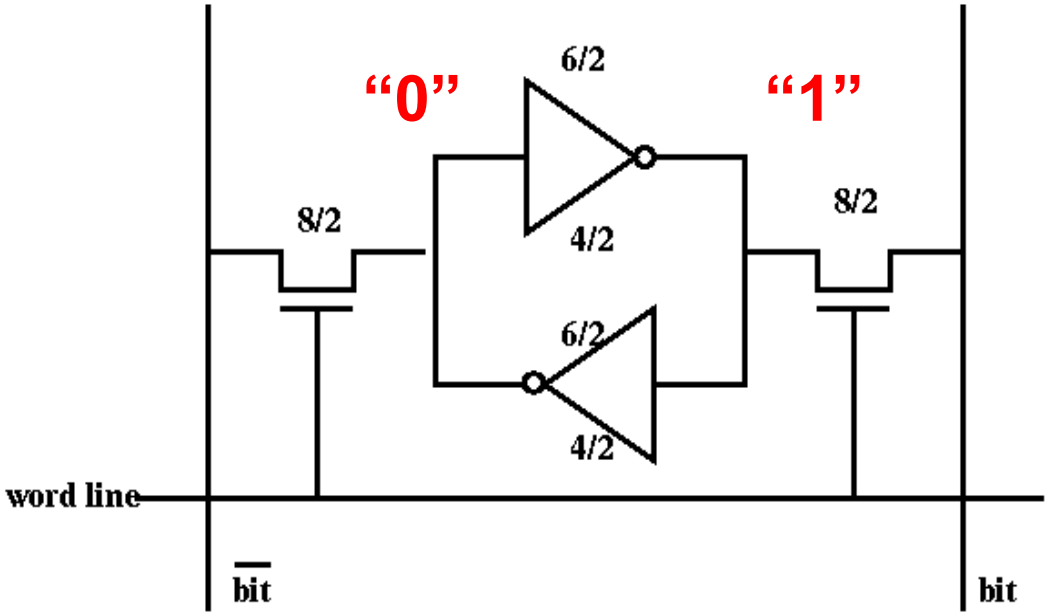
Schemat blokowy pamięci SRAM

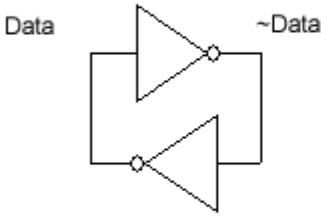


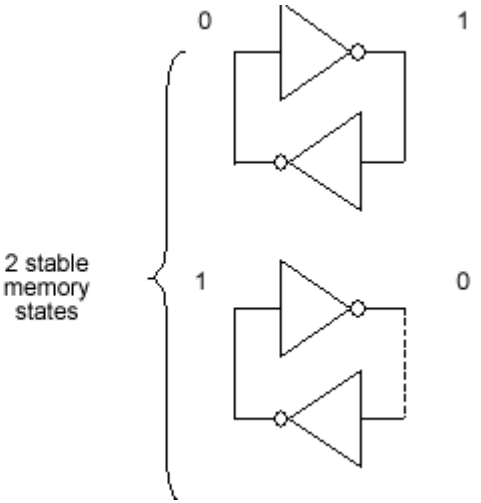
Pin Name	Pin Function
A_0 - A_{19}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1 ~ I/O_4	Data Inputs/Outputs
V_{CC}	Power(+5.0V)
V_{SS}	Ground
N.C	No Connection

Komórka pamięci statycznej

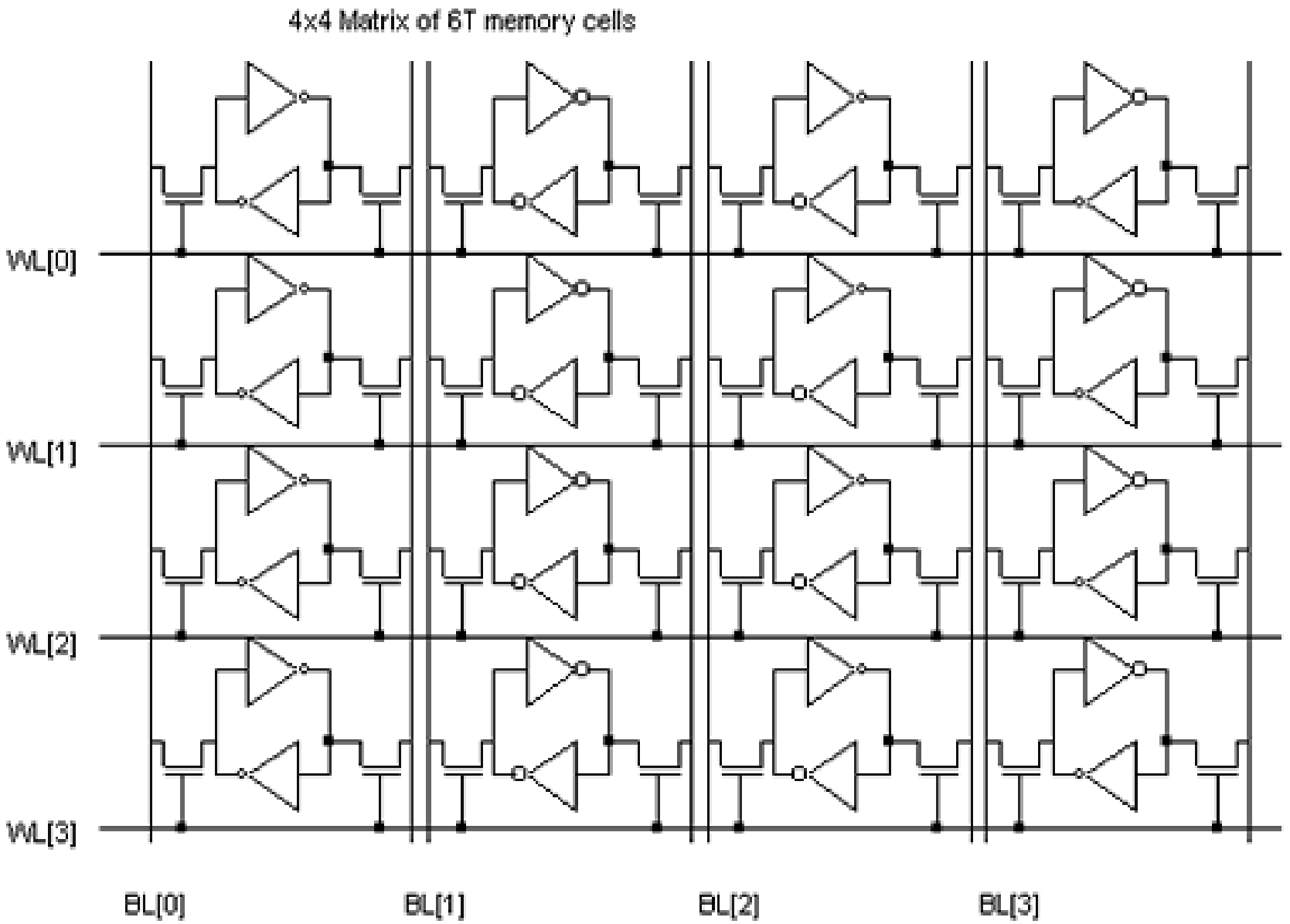








Matryca pamięci statycznej



Pamięci SRAM

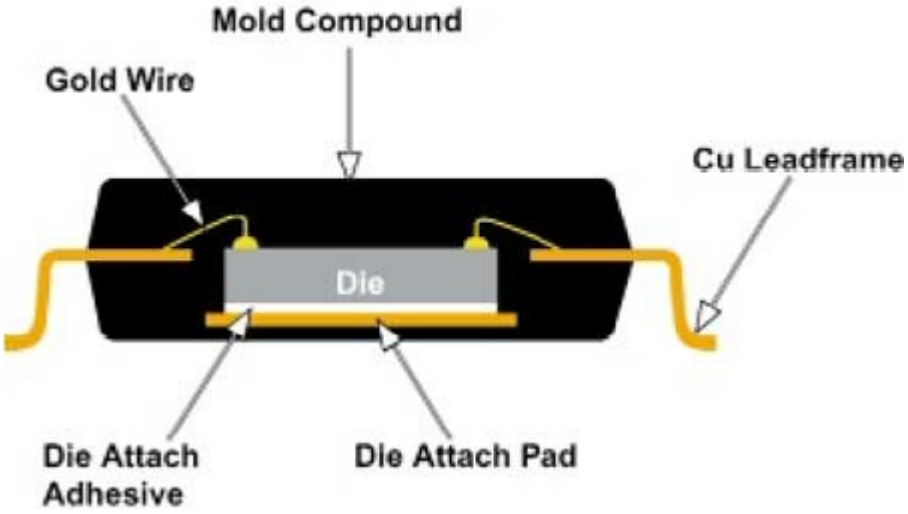
Zalety:

- Szybki czas zapisu oraz odczytu (~10 ns),
- Niskie napięcie zasilania (~1.2V - 5 V),
- Niewielkie rozmiary,
- Mały pobór energii.

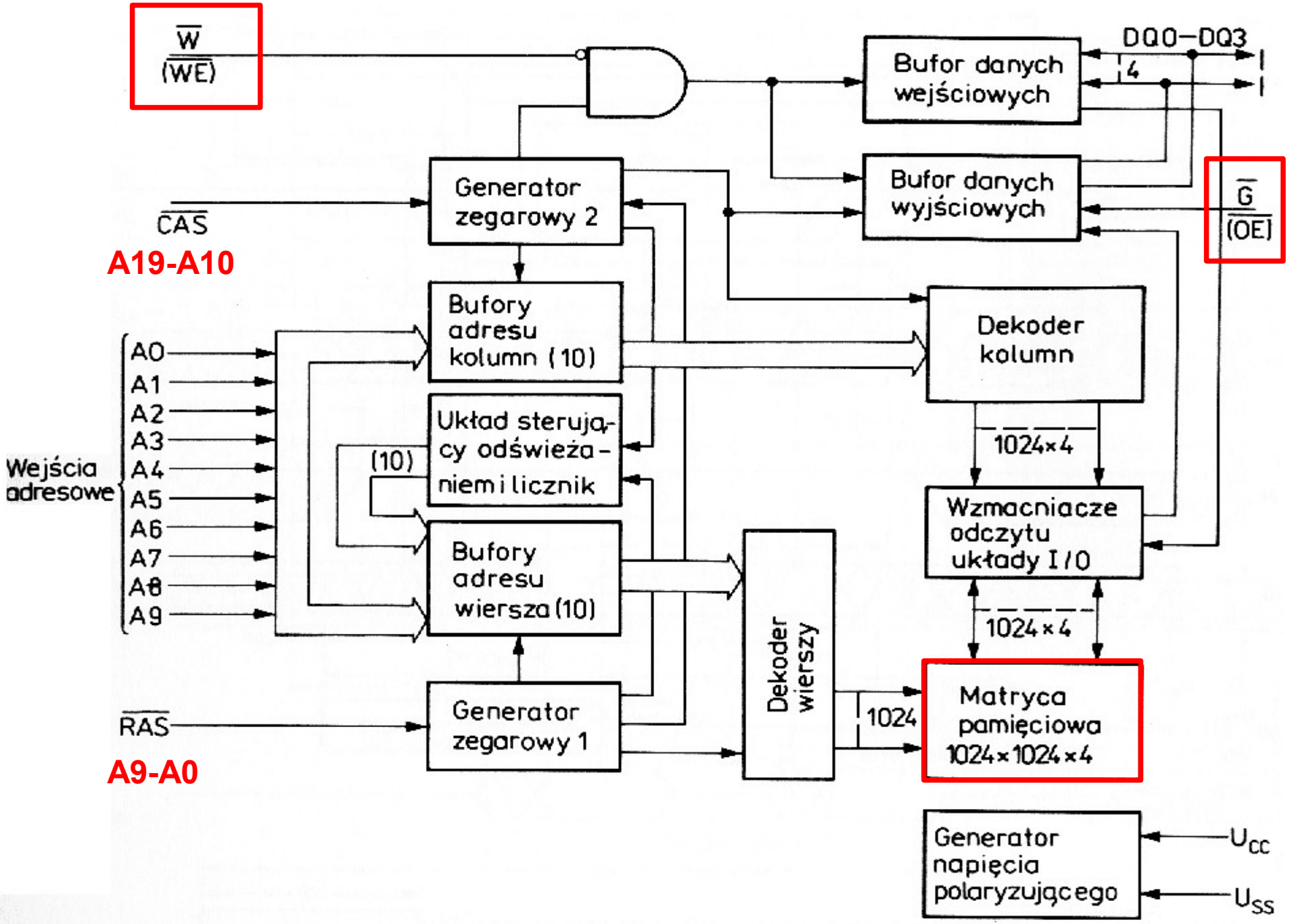
Wady:

- Stosunkowo niewielkie pojemności pamięci (< 4 MB),
- Wysoka cena pamięci.

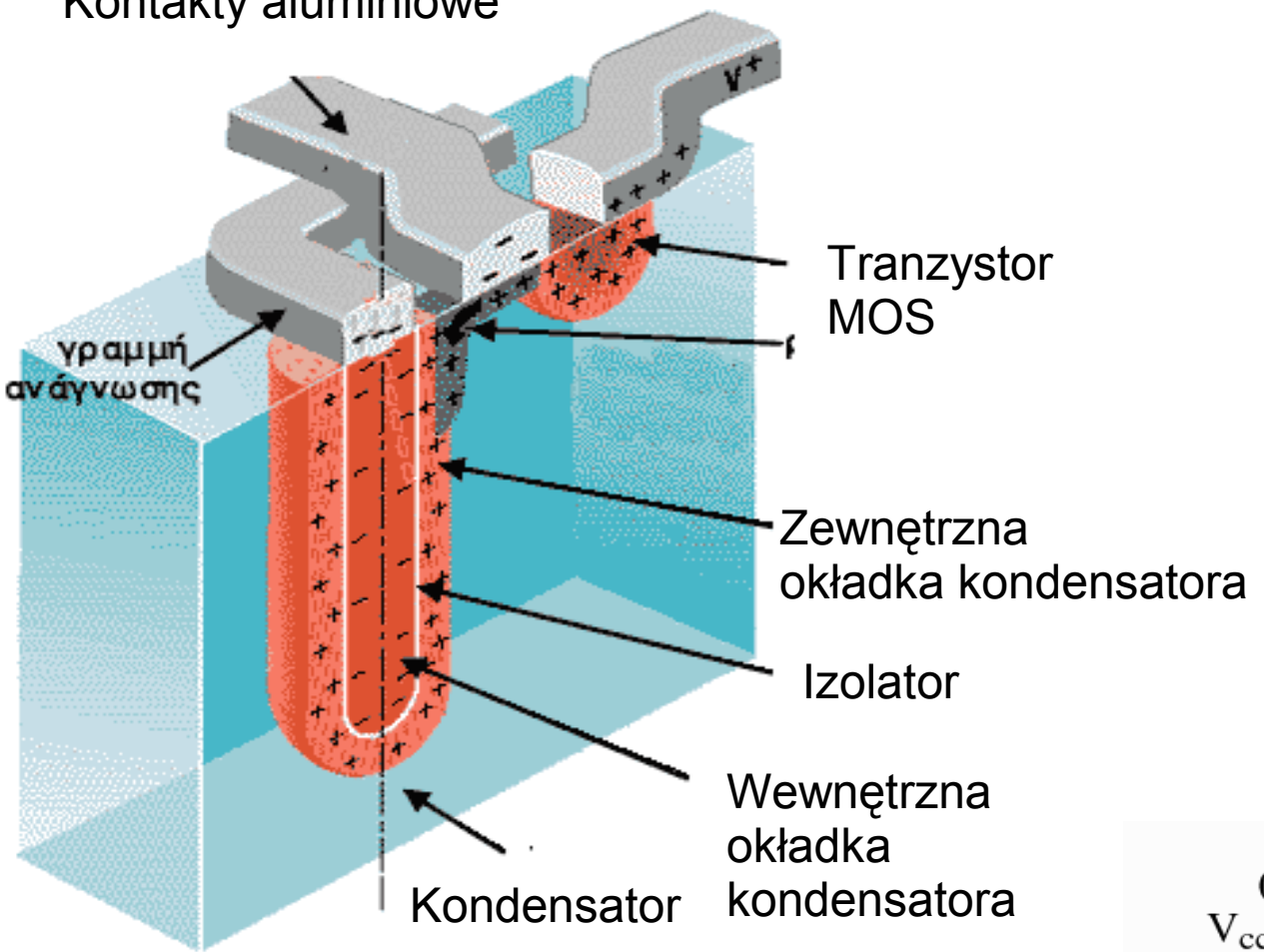
Pamięci statyczne

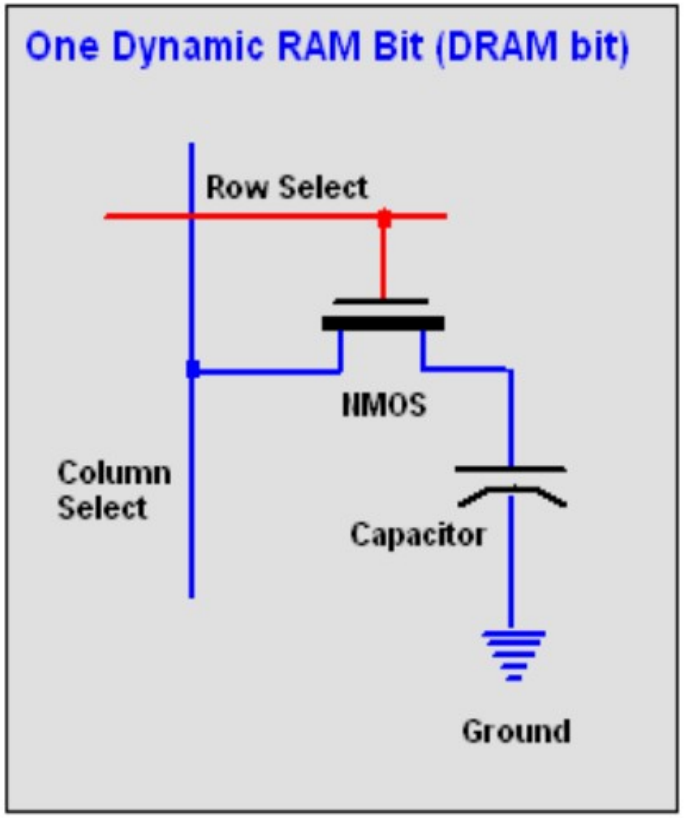


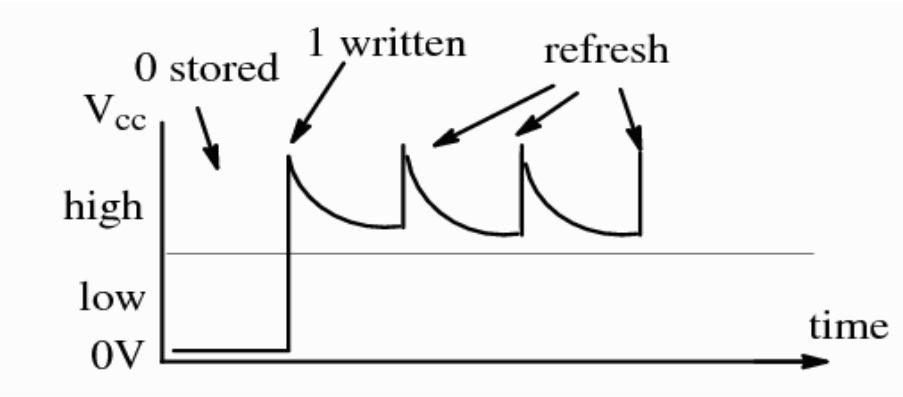
Pamięci dynamiczne DRAM



Komórka pamięci dynamicznej

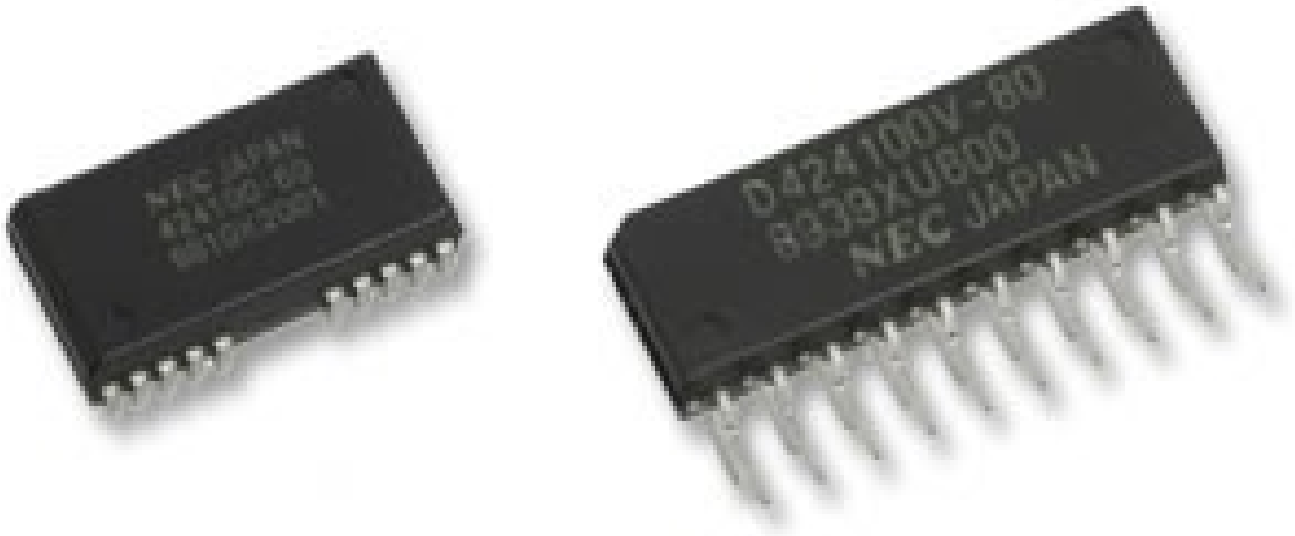


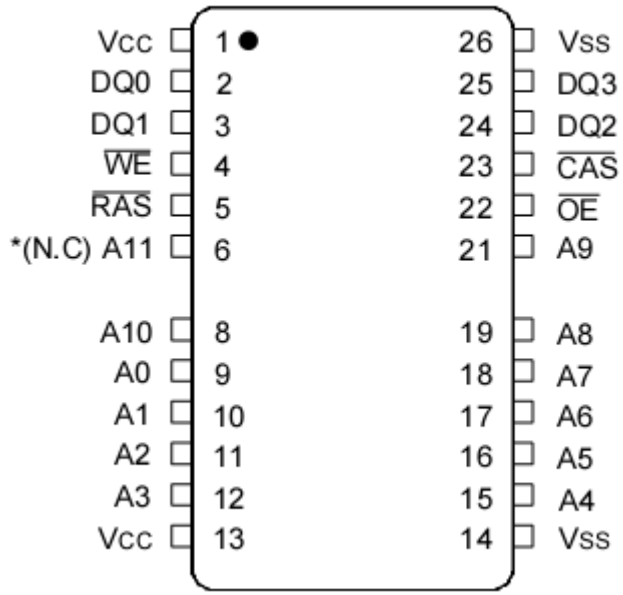




Czas odświeżania: 4 – 16 ms

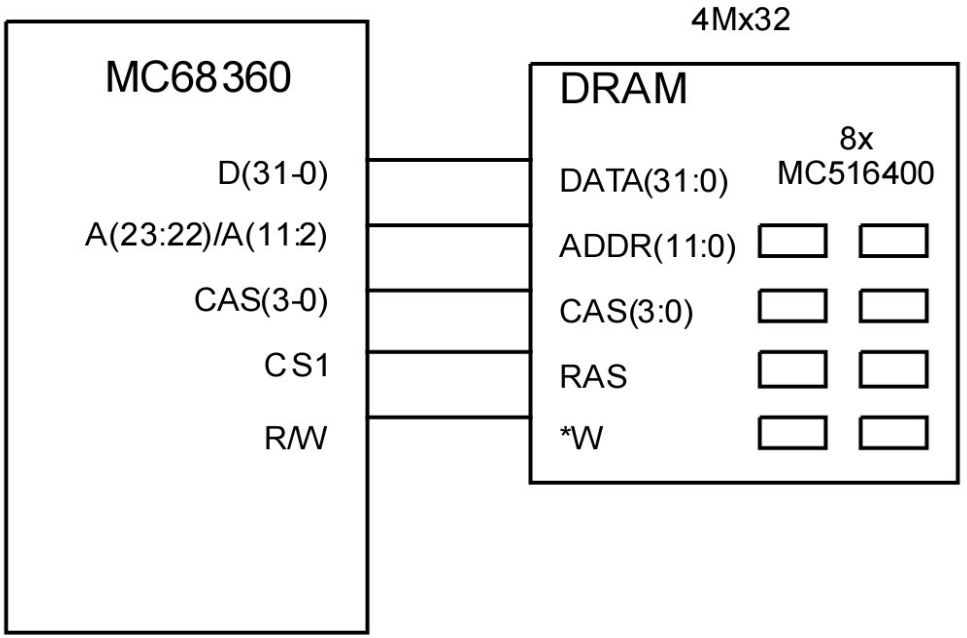
Pamięć DRAM 1 Mx4

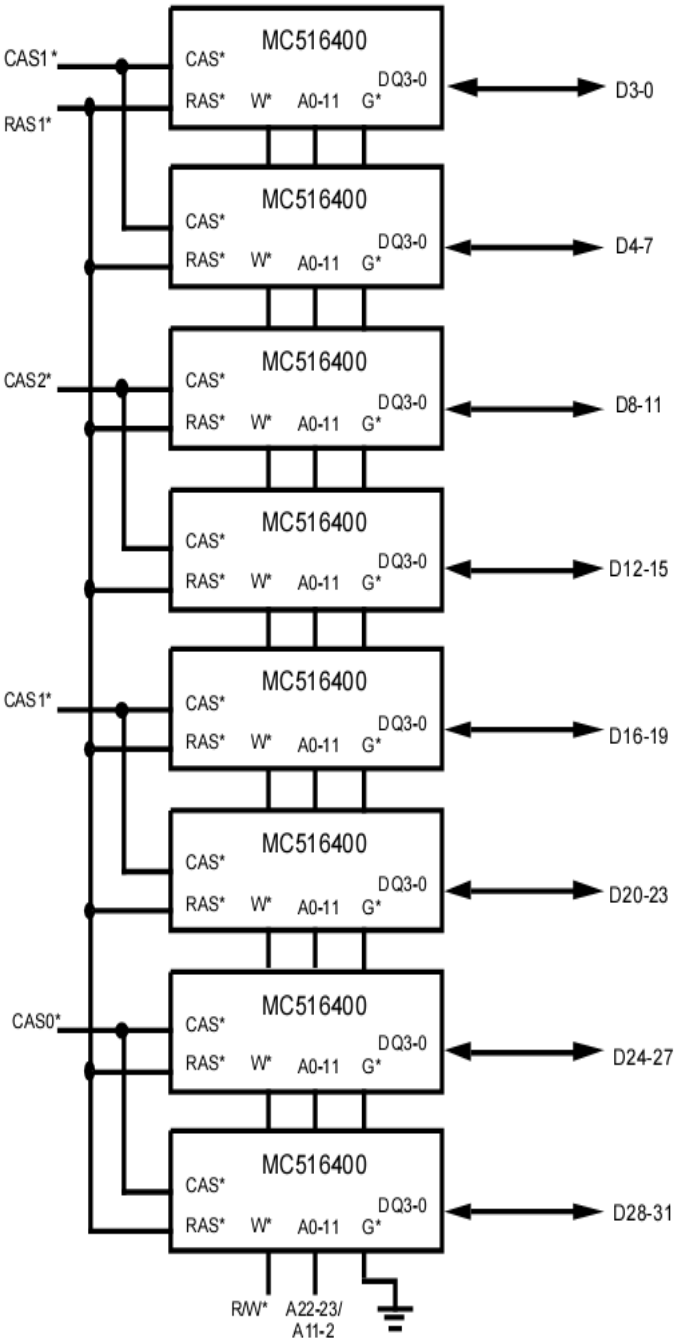




Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A11	Address Input (4K Refresh Product)
A0~A10	Address Input (2K Refresh Product)
DQ0~DQ3	Data In/Out
Vcc	Power (3.3V)
Vss	Ground
NC	No Connection

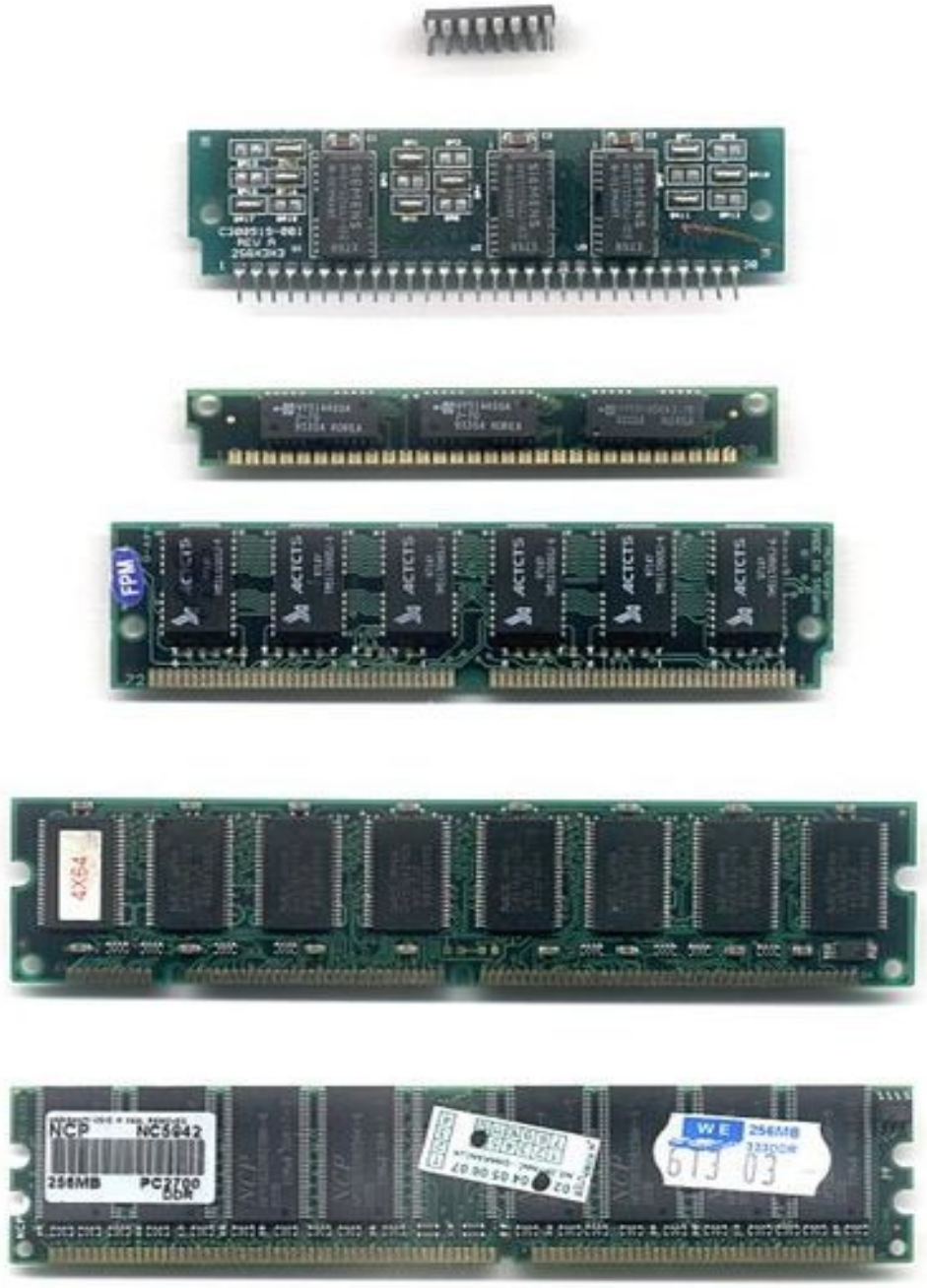
Pamięci 32-bitowe





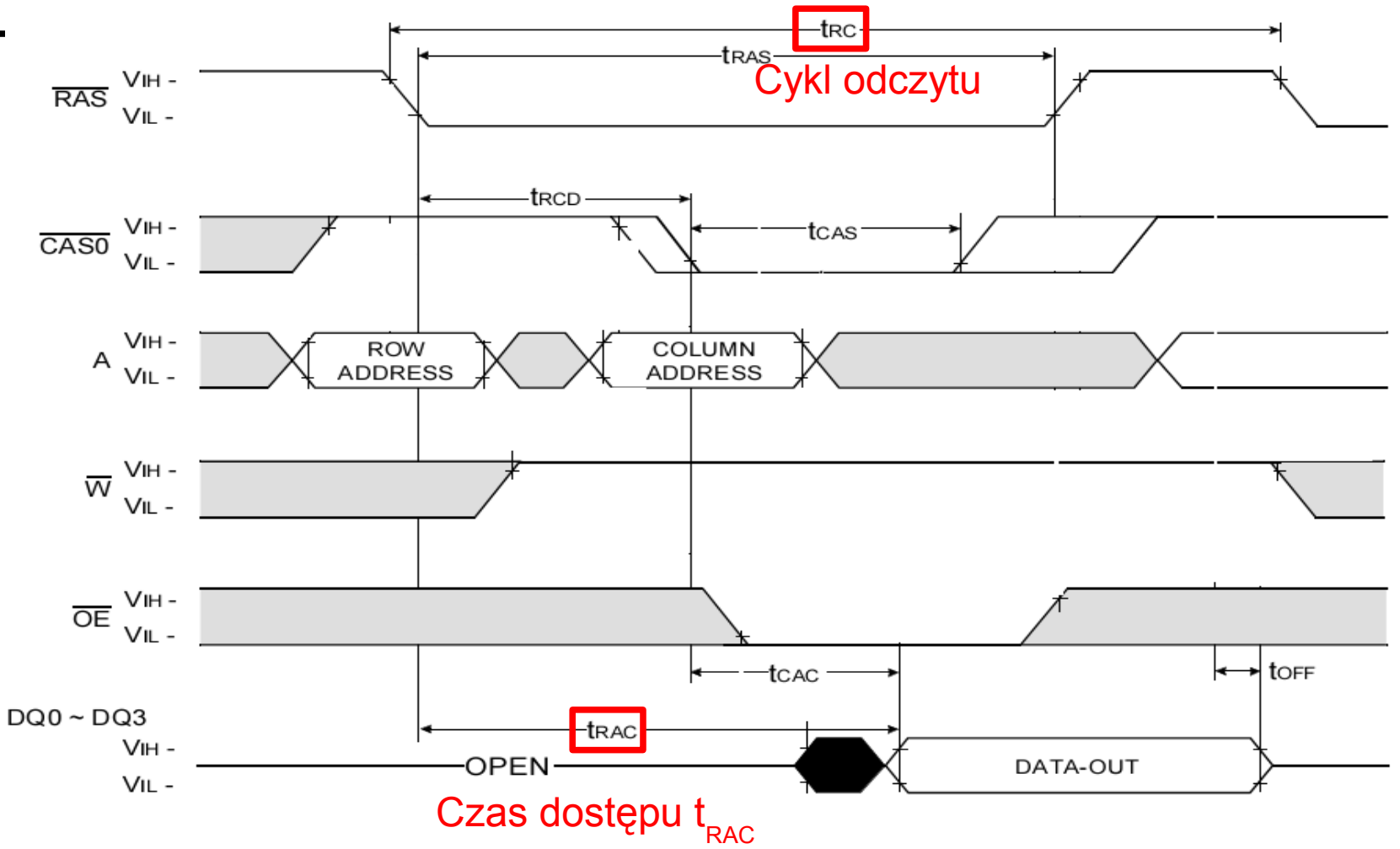
VAX 8600 memory board

Pamięci dynamiczne



Procesor z dwoma pamięciami SDRAM

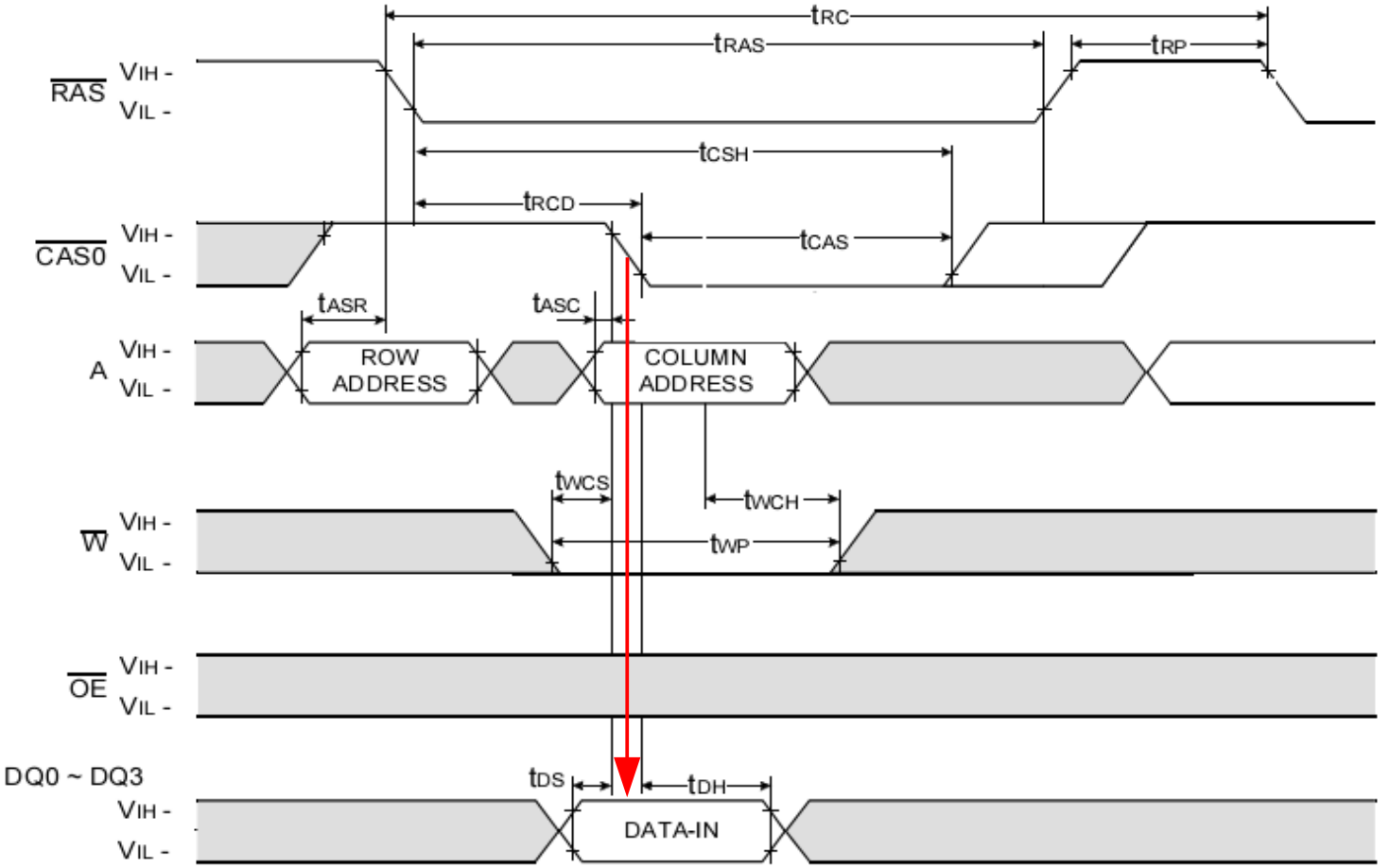
Cykl odczytu z pamięci dynamicznej



Czas dostępu t_{RAC}

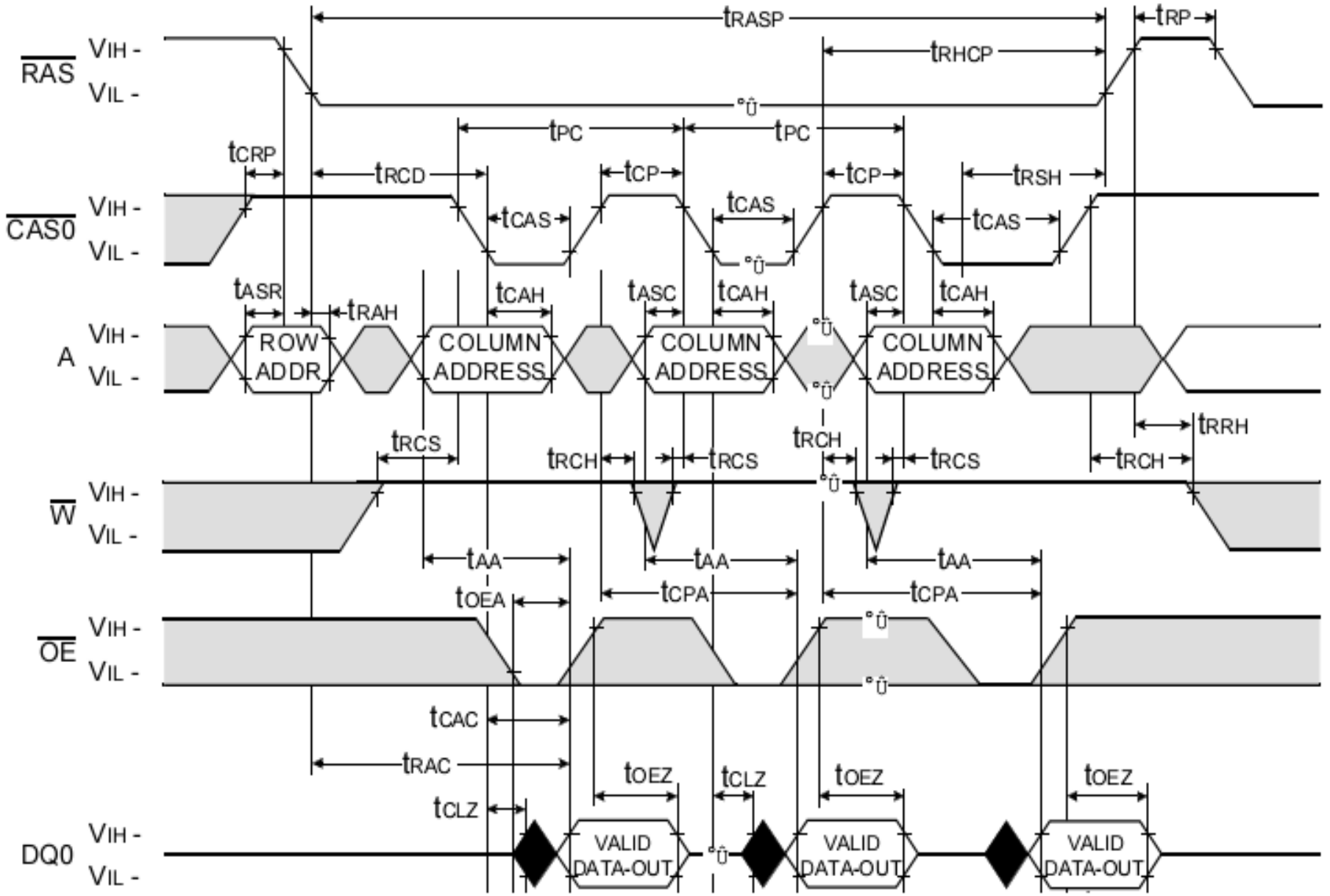
MNEMONIC	SIGNAL NAME	VALUE (ns)
t_{RCD}	Row-to-column strobe lead time	25–75
t_{CAC}	Access time from column address strobe	25 max.
t_{RAC}	Access time from row address strobe	100 max.
t_{OFF}	Output buffer turn off time	0–20

Cykl zapisu do pamięci dynamicznej



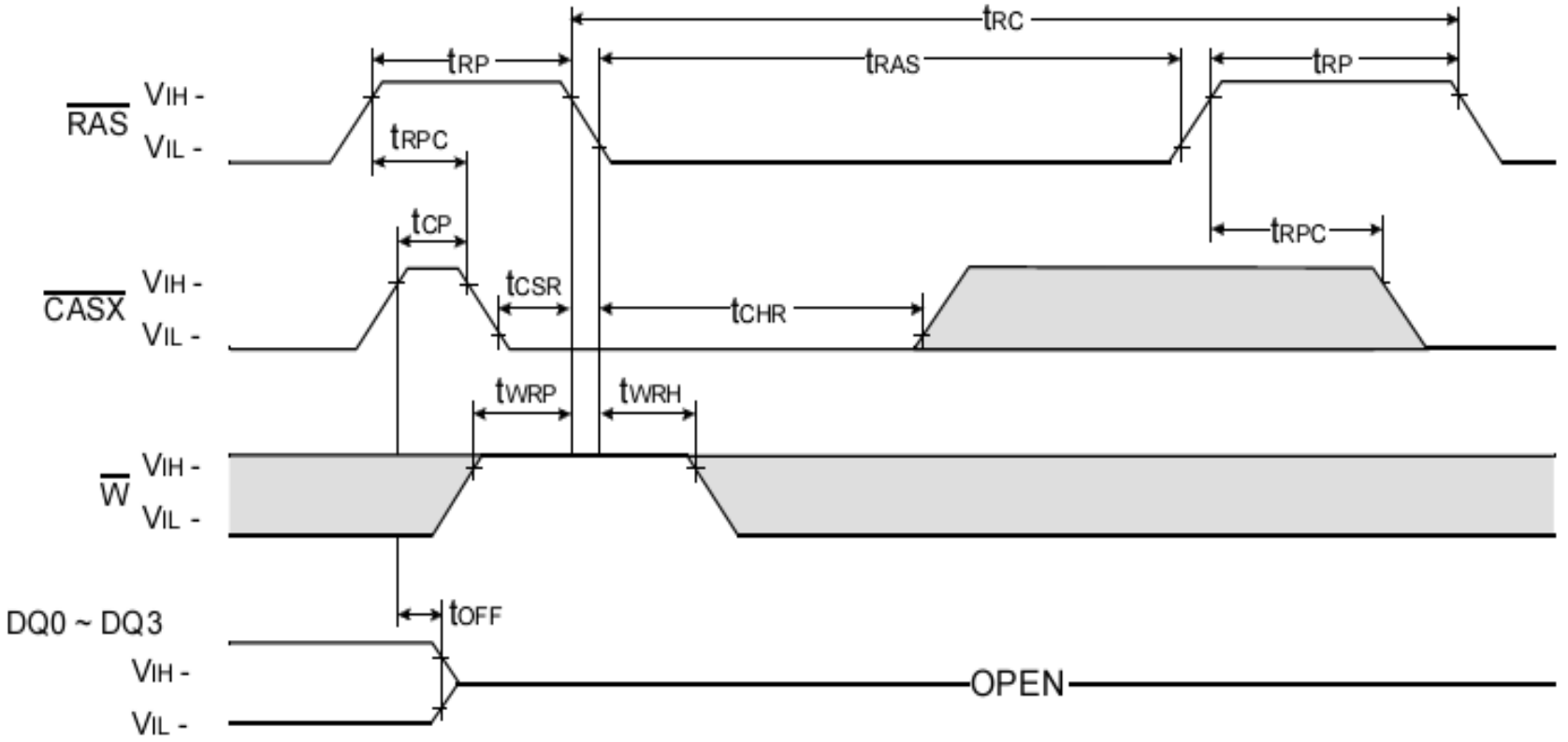
MNEMONIC	NAME	VALUE (ns)
t_{WCS}	Write command setup time	0 min.
t_{WCH}	Write command hold time	20 min.
t_{WP}	Write command pulse width	20 min.
t_{DS}	Data setup time	0 min.
t_{DH}	Data hold time	20 min.

Cykl szybkiego stronicowania (odczyt)



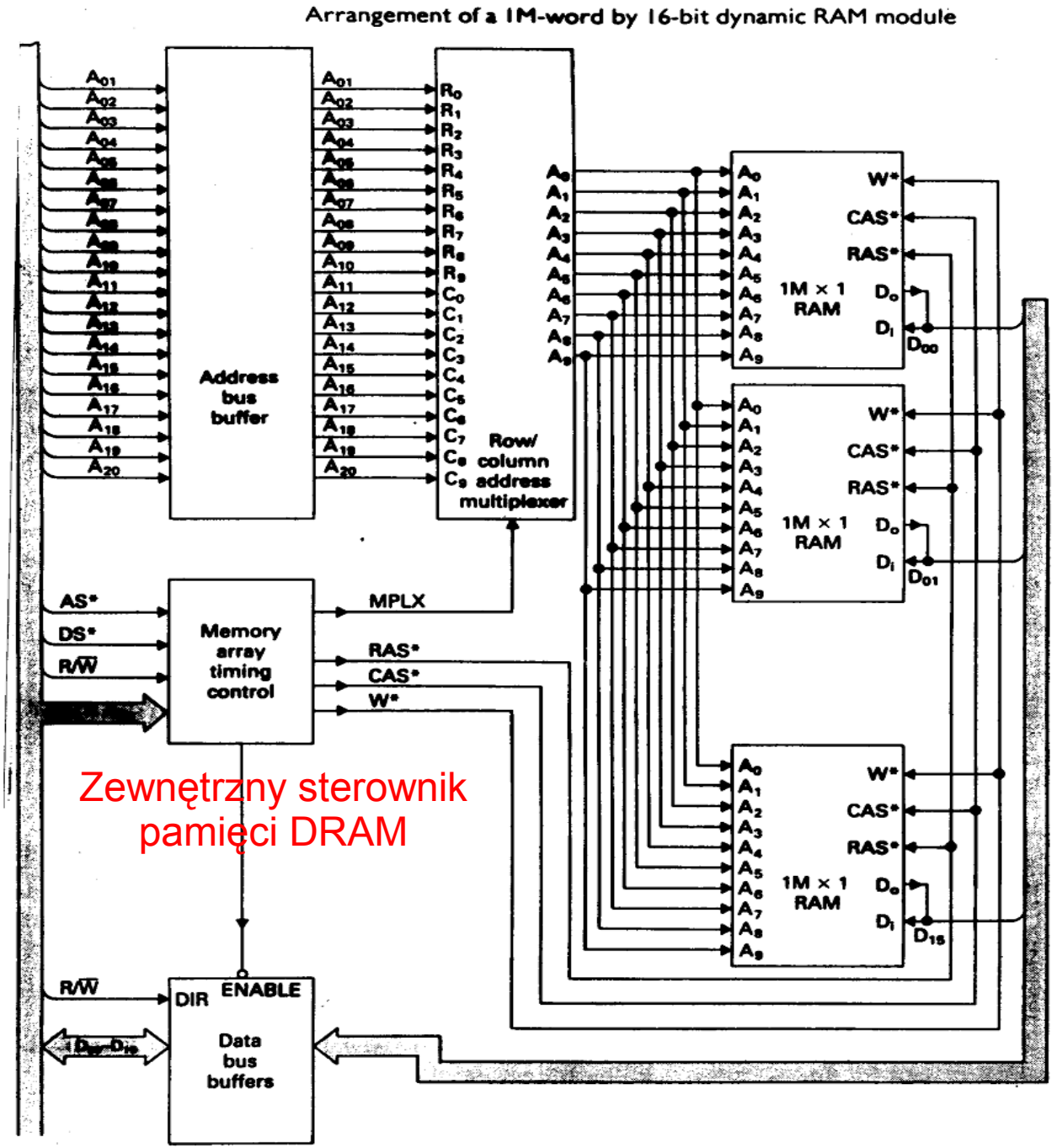
Cykl odświeżania

Odświeżanie typu CAS przed RAS



Pamięć MCM54400A-60 (1 Mx4):
Cykl odświeżania: T_R=16 ms, czas dostępu: t_{RAC}=60 ns, cykl odczytu: t_{RC}=110 ns,
Czas potrzebny na odświeżenie 1024 wierszy: 1024 * 110 ns = 113 us (0,7 % cyklu T_R)

Współpraca pamięci DRAM z procesorem 68k

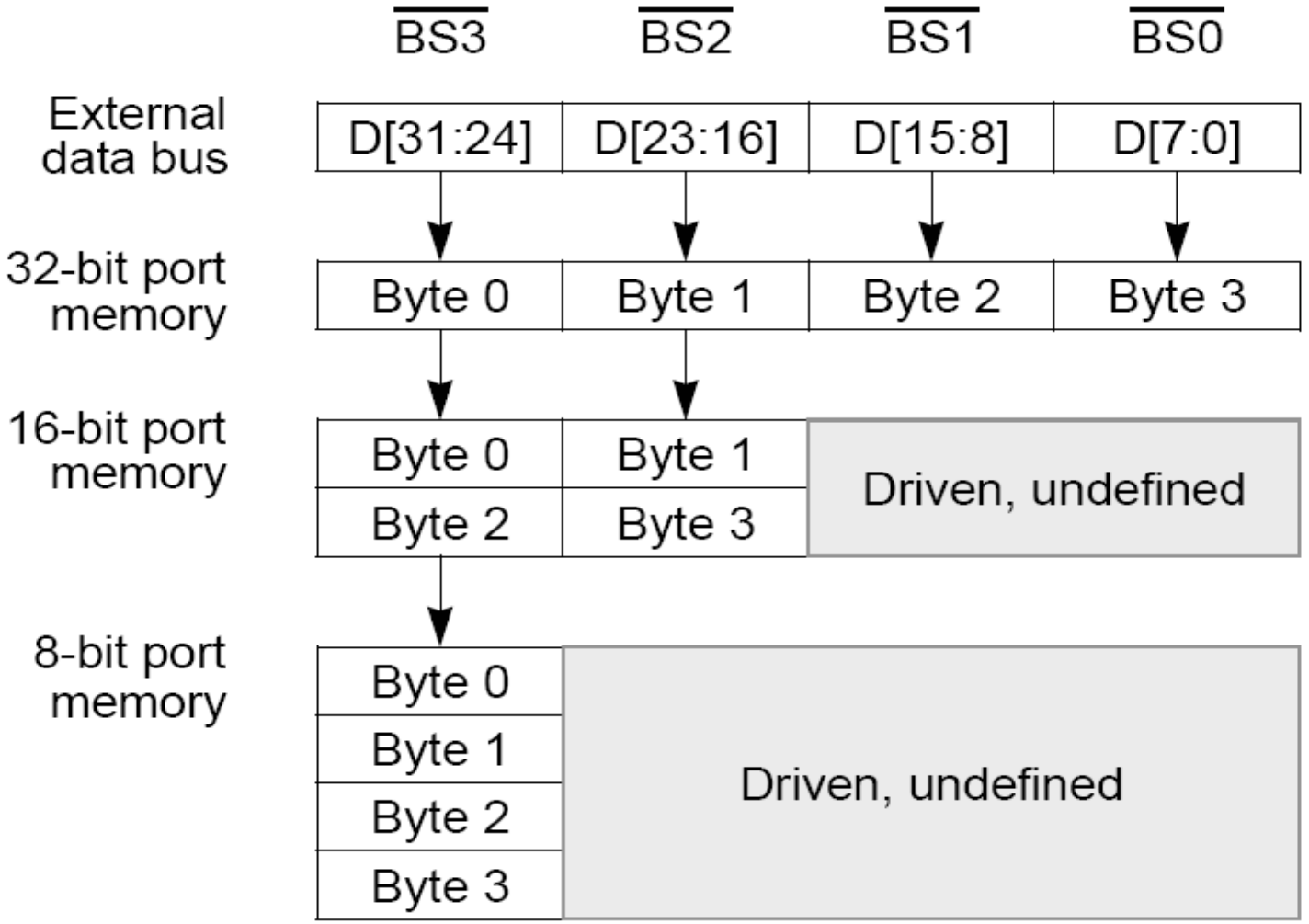


Address strobe
Data strobe
Read/Write

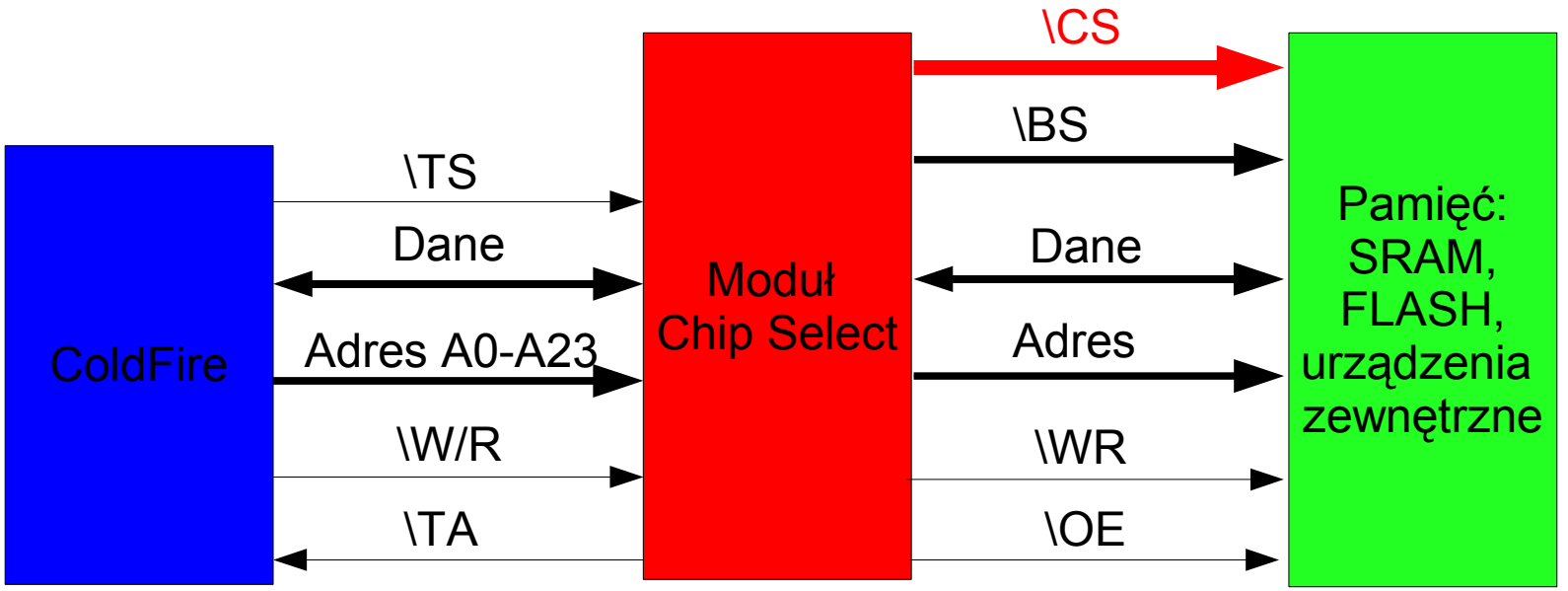
Zewnętrzny sterownik pamięci DRAM

D0-D15

Transfery danych procesora motorola



Moduł sterujący pamięcią procesora Motorola ColdFire



\TA – Transfer Acknowledge, potwierdzenie transmisji
\TS – Transfer Strobe, ważne dane oraz adresy na magistralach
\TIP – Transfer In Progres, utrzymywany w stanie niskim do zakończenia transmisji
\TEA – Transfer Error, wejście sygnalizacji błędu zewnętrznego

Rejestry konfiguracyjne

Chip Select Address Registers (CSAR0–CSAR6)

Bits	Name	Description
15–0	BA	Base address. Defines the base address for memory dedicated to chip select $\overline{\text{CS}}$[6:0]. BA is compared to bits 31–16 on the internal address bus to determine if chip select memory is being accessed.

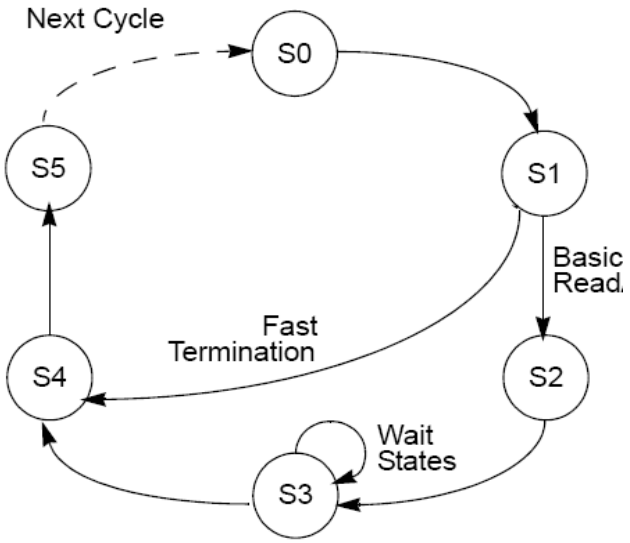
Chip Select Mask Registers (CSMR0–CSMR6)

	31 … 16	15 … 9	8	7	6	5	4	3	2	1	0
Field	BAM	—	WP	—	AM	C/I	SC	SD	UC	UD	V
Reset	Unitialized										0
R/W	R/W										
Addr	0x084 (CSMR0); 0x090 (CSMR1); 0x09C (CSMR2); 0x0A8 (CSMR3); 0x0B4 (CSMR4); 0x0C0 (CSMR5); 0x0CC (CSMR6)										

Chip Select Control Registers (CSCR0–CSCR6)

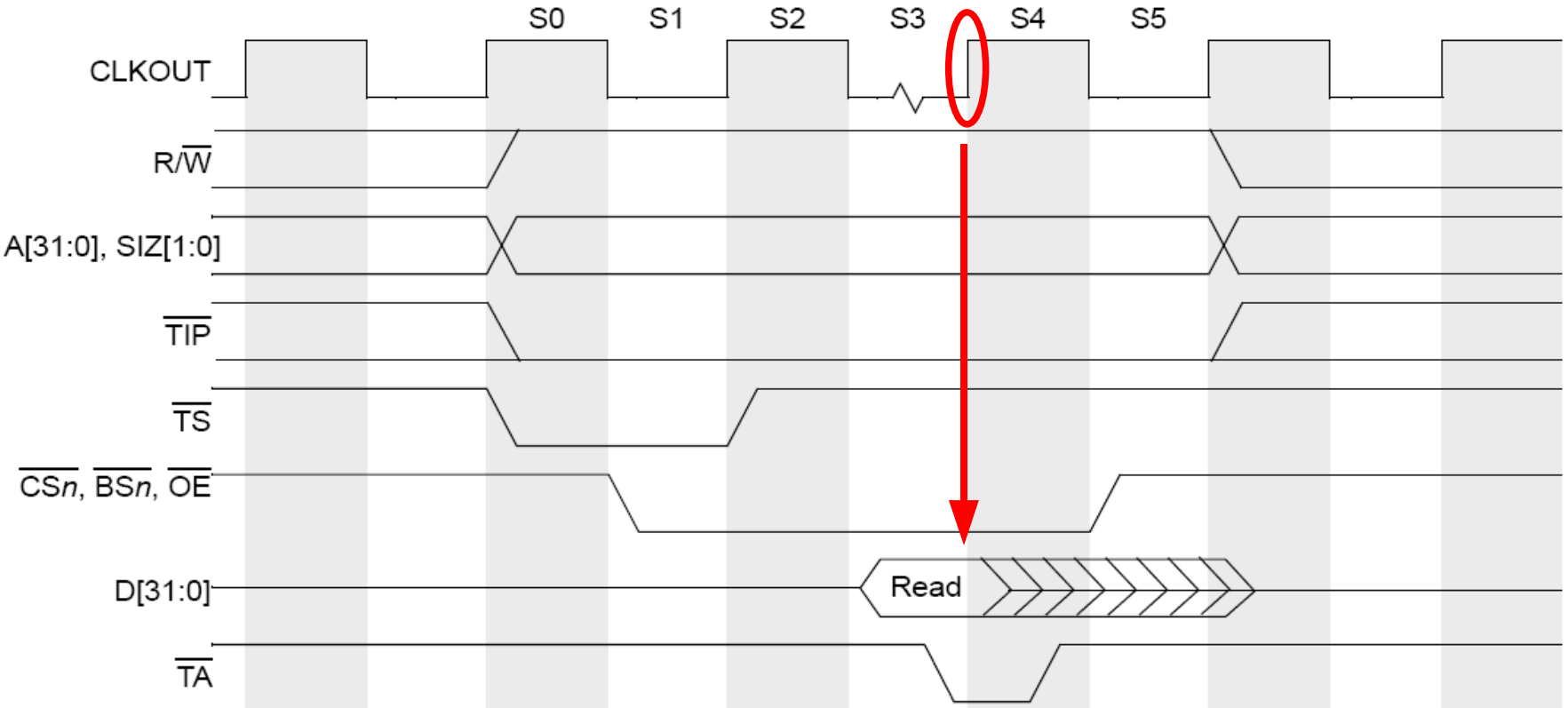
Bits	Name	Description
15–14	—	Reserved, should be cleared.
13–10	WS	Wait states. The number of wait states inserted before an internal transfer acknowledge is generated (WS = 0 inserts zero wait states, WS = 0xF inserts 15 wait states). If AA = 0, $\overline{TA}$ must be asserted by the external system regardless of the number of wait states generated. In that case, the external $\overline{TA}$ transfer acknowledge ends the cycle. An external $\overline{TA}$ supercedes the generation of an internal $\overline{TA}$.
9	—	Reserved, should be cleared.
8	AA	Auto-acknowledge enable. Determines the assertion of the internal transfer acknowledge for accesses specified by the chip select address. 0 No internal $\overline{TA}$ is asserted. Cycle is terminated externally. 1 Internal $\overline{TA}$ is asserted as specified by WS. Note that if AA = 1 for a corresponding $\overline{CS}n$ and the external system asserts an external $\overline{TA}$ before the wait-state countdown asserts the internal $\overline{TA}$, the cycle is terminated. Burst cycles increment the address bus between each internal termination.
7–6	PS	Port size. Specifies the width of the data associated with each chip select. It determines where data is driven during write cycles and where data is sampled during read cycles. See Section 12.3.1.1. 00 32-bit port size. Valid data sampled and driven on D[31:0] 01 8-bit port size. Valid data sampled and driven on D[31:24] 1x 16-bit port size. Valid data sampled and driven on D[31:16]
5	BEM	Byte enable mode. Specifies the byte enable operation. Certain SRAMs have byte enables that must be asserted during reads as well as writes. BEM can be set in the relevant CSCR to provide the appropriate mode of byte enable in support of these SRAMs. 0 $\overline{BS}$ is not asserted for read. $\overline{BS}$ is asserted for data write only. 1 $\overline{BS}$ is asserted for read and write accesses.
4	BSTR	Burst read enable. Specifies whether burst reads are used for memory associated with each $\overline{CS}n$. 0 Data exceeding the specified port size is broken into individual, port-sized non-burst reads. For example, a longword read from an 8-bit port is broken into four 8-bit reads. 1 Enables data burst reads larger than the specified port size, including longword reads from 8- and 16-bit ports, word reads from 8-bit ports, and line reads from 8-, 16-, and 32-bit ports.
3	BSTW	Burst write enable. Specifies whether burst writes are used for memory associated with each $\overline{CS}n$. 0 Break data larger than the specified port size into individual port-sized, non-burst writes. For example, a longword write to an 8-bit port takes four byte writes. 1 Enables burst write of data larger than the specified port size, including longword writes to 8 and 16-bit ports, word writes to 8-bit ports and line writes to 8-, 16-, and 32-bit ports.
2–0	—	Reserved, should be cleared.

Cykl odczytu (ColdFire)

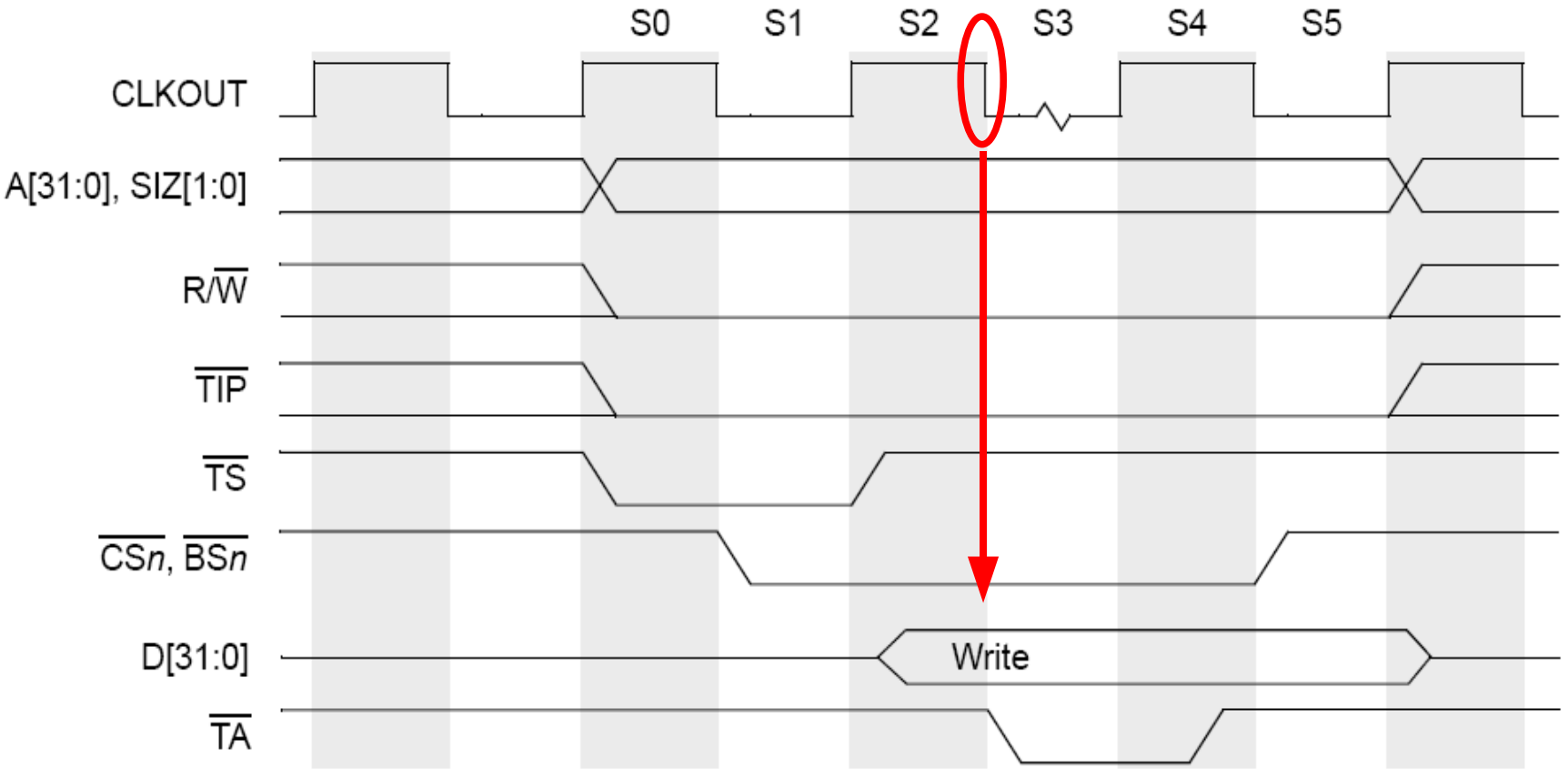


SIZ[1:0]	Transfer Size
00	Longword
01	Byte
10	Word
11	16-byte line

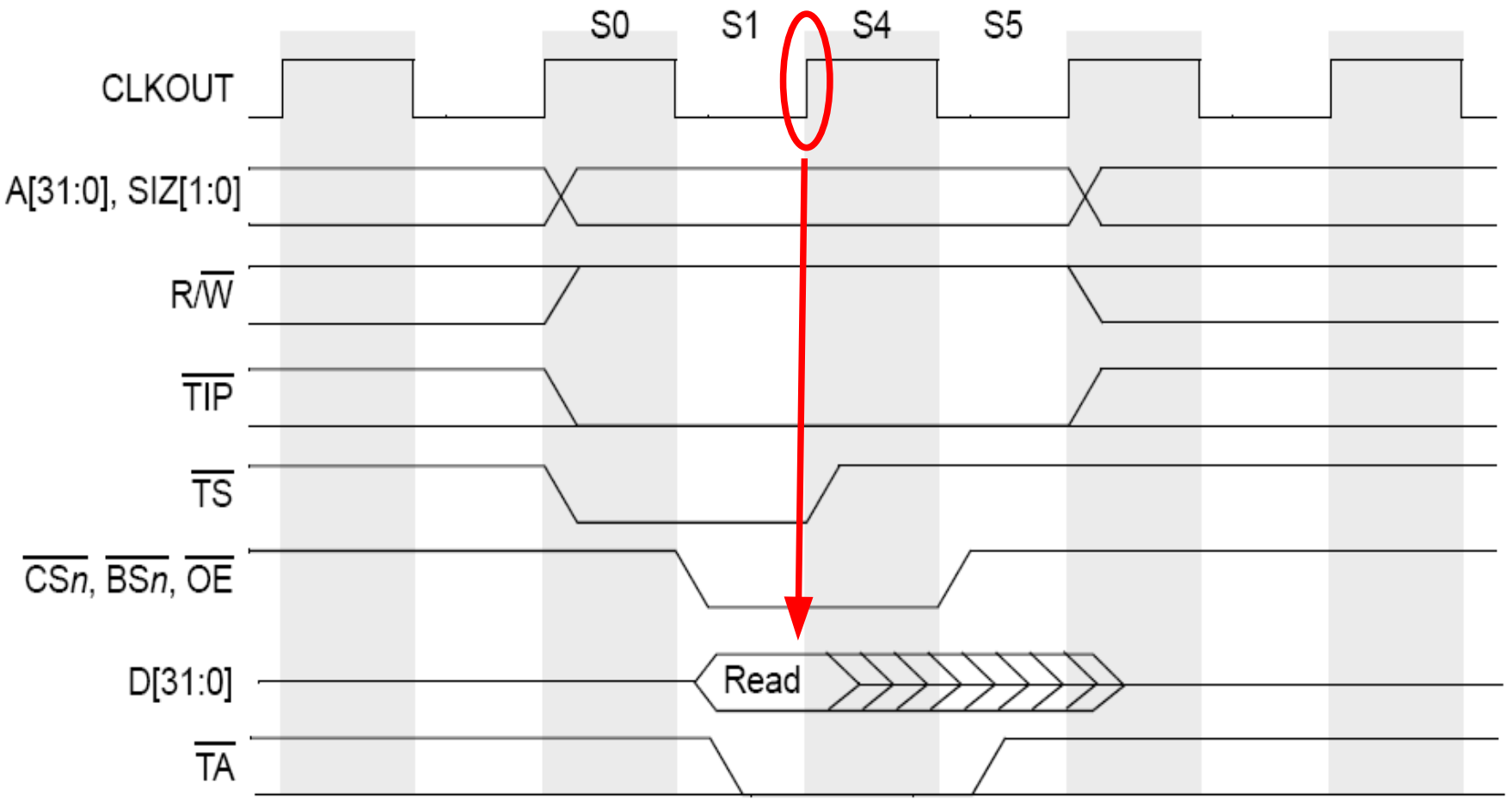
Narastające zbocze zegara



Podstawowy cykl zapisu (ColdFire)

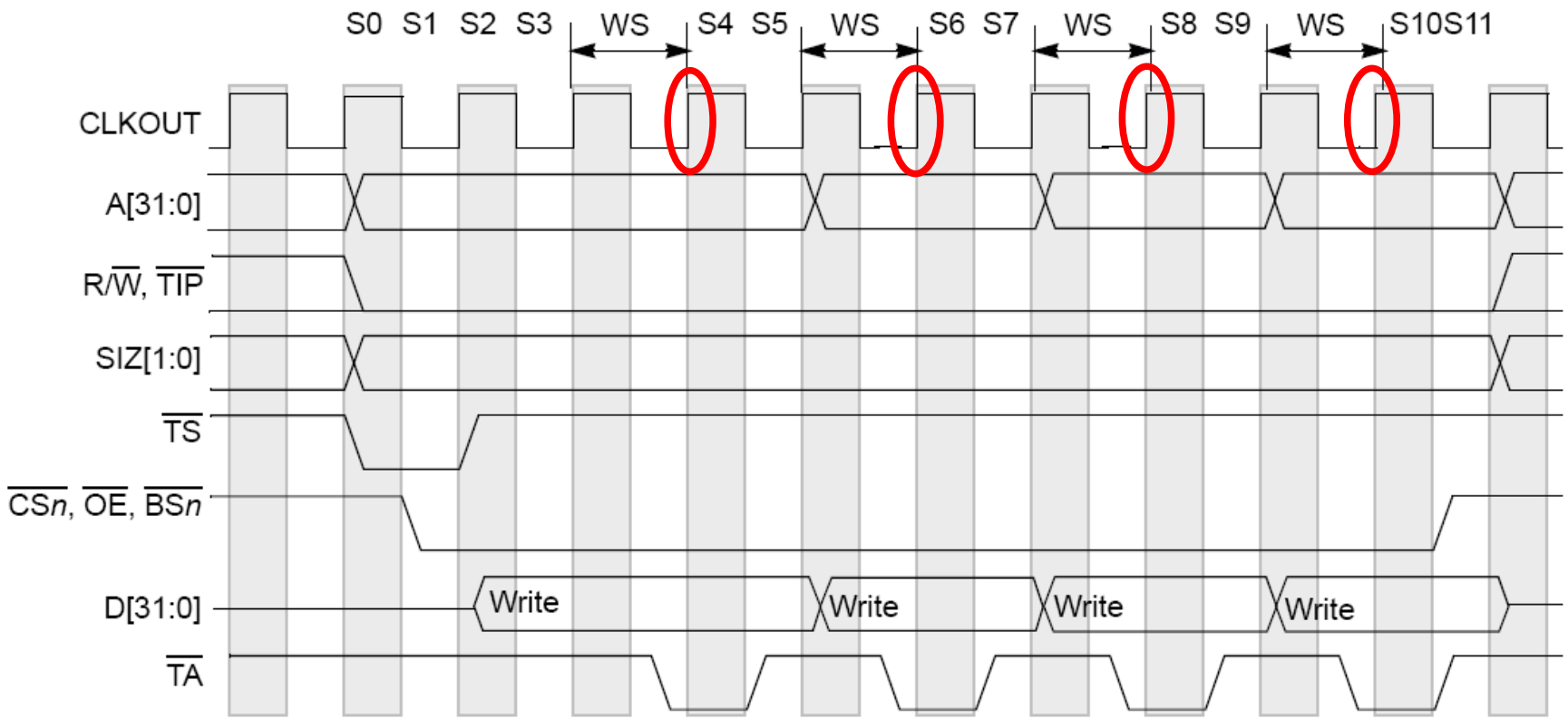


Cykl odczytu z szybkim zakończeniem (ColdFire)



Tryb z szybkim zakończeniem nie może zostać użyty podczas wewnętrznej terminacji.

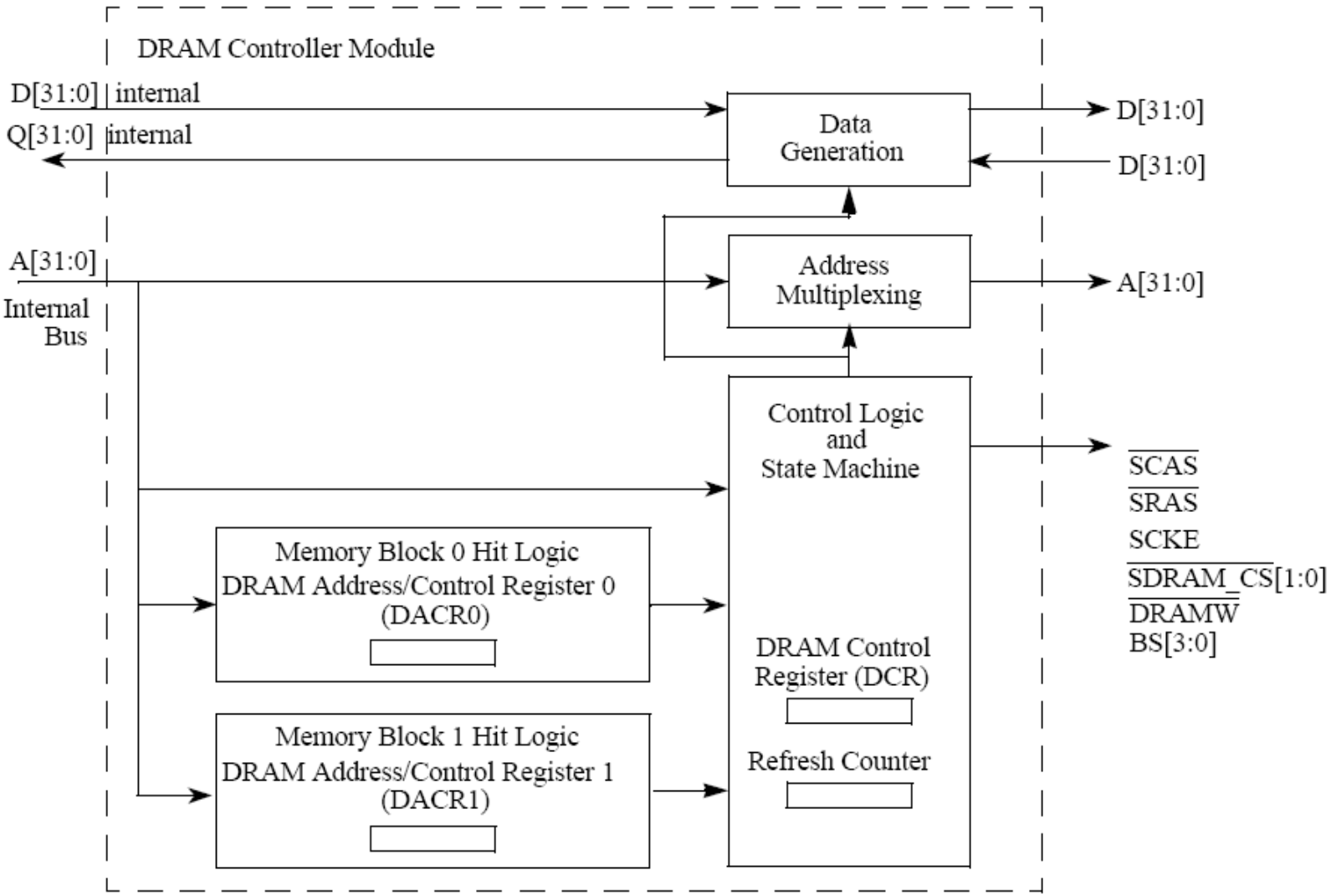
Cykl zapisu burst (3-2-2-2) (ColdFire)



Cykle zapisu i odczytu wykorzystywane podczas transmisji DMA oraz operacji na pamięci podręcznej.

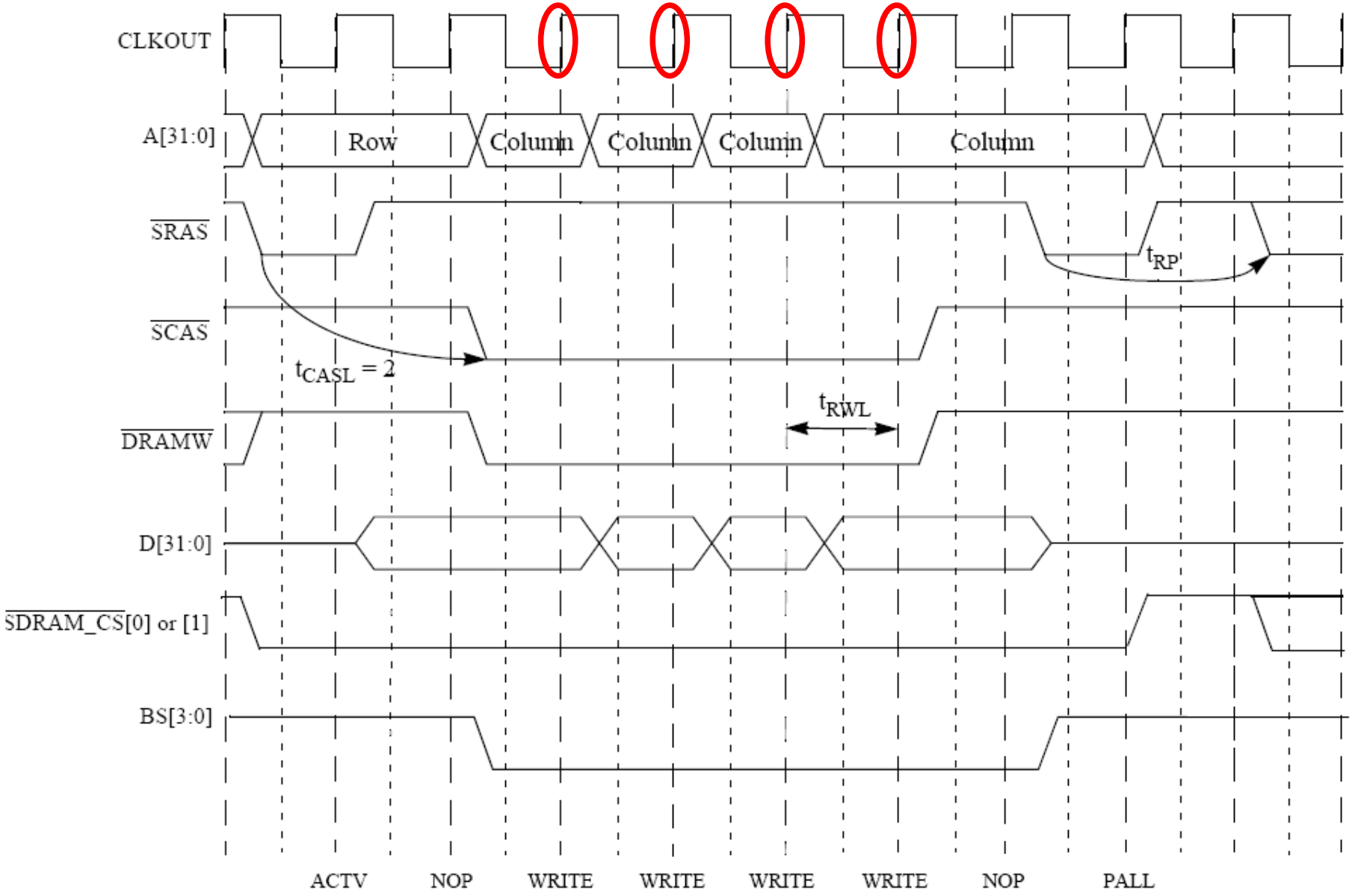
Sterownik pamięci dynamicznej

- Obsługa dwóch pamięci dynamicznych SDRAM MCF528x (MCF520x/MCF527x pamięci DDR)
- Programowalne linie SRAS, SCAS oraz czas odświeżania
- Obsługa pamięci 8, 16, 32 bitowych



Transmisja zapisu do pamięci SDRAM

Transfer typu burst



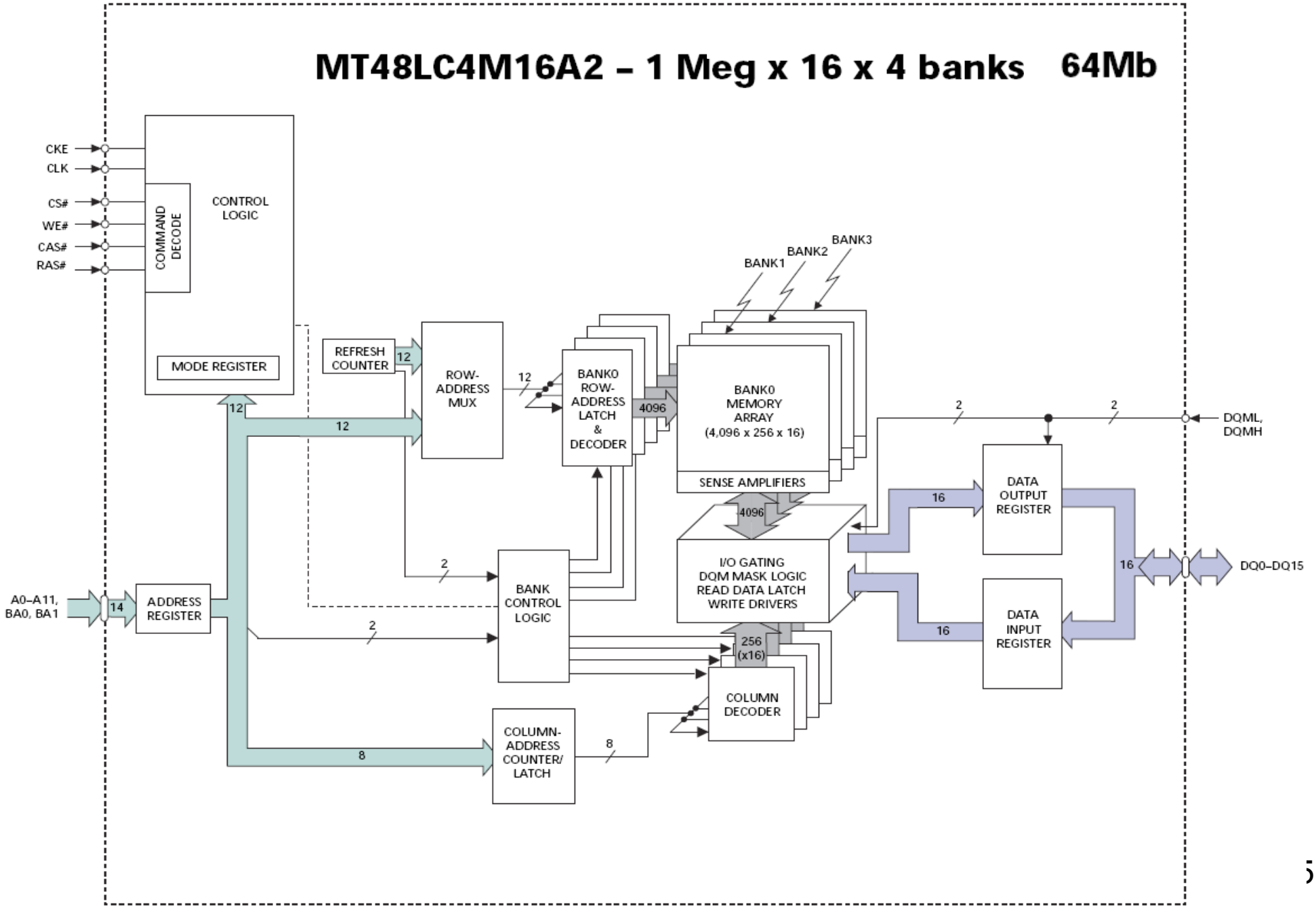
Rejestry konfiguracyjne

IPSBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x040	DRAM control register (DCR) [p. 15-5]		—	
0x044	—			
0x048	DRAM address and control register 0 (DACR0) [p. 15-6]			
0x04C	DRAM mask register block 0 (DMR0) [p. 15-8]			
0x050	DRAM address and control register 1 (DACR1) [p. 15-6]			
0x054	DRAM mask register block 1 (DMR1) [p. 15-8]			

	16 Meg x 4	8 Meg x 8	4 Meg x 16
Configuration	4 Meg x 4 x 4 banks	2 Meg x 8 x 4 banks	1 Meg x 16 x 4 banks
Refresh count	4K	4K	4K
Row addressing	4K (A0–A11)	4K (A0–A11)	4K (A0–A11)
Bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column addressing	1K (A0–A9)	512 (A0–A8)	256 (A0–A7)

Parameter	Specification
Speed grade (-6)	166 MHz
12 rows, 8 columns	
Two bank-select lines to access four internal banks	
ACTV-to-read/write delay (t_{RCD})	18 ns (min.)
Period between auto-refresh and ACTV command (t_{RC})	60 ns
ACTV command to precharge command (t_{RAS})	42 ns (min.)
Precharge command to ACTV command (t_{RP})	18 ns (min.)
Last data input to PALL command (t_{RWL})	1 bus clock
Auto-refresh period for 4096 rows (t_{REF})	64 ms

Pamięć SDRAM firmy Micron



Dołączenie pamięci SDRAM Micron 64 Mbit do procesora MCF5282

MCF5282 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22	A23
Row	15	14	13	12	11	10	9	17	18	19	20	21	22	23
Column	2	3	4	5	6	7	8	16						
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	**BA0**	**BA1**